CURRICULUM VITAE

SARIN VIJAY MYTHRY
Door no: 5-8-124/75,
Narayana Reddy Colony,
Sangareddy,
Telangana State-502001.

Mobile No: 09963515176,9133318282
Mail: sarinmythry@gmail.com

CAREER OBJECTIVE:

Seeking a career in an organization that enables me to utilize my skills and abilities while giving me an opportunity for professional growth.

ACADEMIC PROFILE:

- **Ph.D [ECE] :** Karunya University, Coimbatore.
- **M.E [ECE] :** Karunya University, Coimbatore.
- **B.Tech[EEE] :** Ellenki College of Engineering & Technology (JNTUH).
- **XII class :** Guntur Vikas Jr College (BIE), Hyderabad.
- **X class :** MNR Group of Institutions, Hyderabad.
- **GATE Qualified**
- **Successfully completed Seven Courses under NPTEL SWAYAM Program**
- **JNTUH Ratified Faculty Registration ID: 3768-160306-152245**

TECHNICAL SKILLS:

- **Hardware description Languages**:
  VHDL
  Verilog

- **Logic Design Tools:**
  Xilinx Vivado
  Modelsim 6.2g
  Quartus II 9.1

- **Electronic Design Automation Tools:**
  Cadence Virtuoso
  Synopsys
  Mentor Graphics
  Tanner EDA
  Micro wind
  DSch
  LT Spice

PERSONAL INFORMATION:

- **Strengths:**
  A Sincere team member, with hard working ability and a capability of working to deadlines.

- **Abilities:**
  Good analytical skills, Logical thinking, Ability to quick grasping and apply new concepts and passion for learning new techniques

ACADEMIC PROJECT (B.Tech):

Title : **Design aspects of Turbo-generator with Standard stipulations**.

Place : BHEL, Hyderabad.

Team Size : 4.

Role : Team Leader.

ACADEMIC PROJECT (M.E):

Title : **Low Power Design of Sinusoidal Clock CBS_ip Triggered Flip-Flop.**

Place : Karunya University, Karunya Nagar, Coimbatore.

Team Size : 1

Title (Mini) : 1.Low Power Design of Double-Edge Triggered Flip-Flop by Reducing the Number of Clocked Transistors.
2.Power Minimization in DET Flip-Flops using reduced number of Transistors.
3.High speed, Low Power and Glitch free CBS_IP technique in Flip Flops.

Place : Karunya University, Karunya Nagar, Coimbatore.

Team Size : 1

RESEARCH PUBLICATIONS:

Sarin Vijay Mythry, D. Jackuline Moni "Low Power Circuits for Recording Human Electrical Signals" Elsevier Integration-VLSI journal [UNDER REVIEW]

[1]. Sarin Vijay Mythry, et al "CMOS ECG amplifier for heart rate analyzer sensor node used in Biomedical IOT applications" IEEE AICTE sponsored 2nd International Conference on Advances in Computing, Communication, Embedded and Secure Systems (ACCESS' 21) held at Adi Shankara Institute of Engineering and Technology, Kalady, Kerala, during Sept.02-04, 2021. [Scopus Indexed]

[2]. Sarin Vijay Mythry, D.Jackuline Moni "A Bulk Driven Buffer Biased Gain Boosted Amplifier for Biomedical Signal Enhancement" Cogent Engineering (Taylor and Francis), Article: 1658966, 12 Sep 2019. [WoS & Scopus Indexed]

[3]. Sarin Vijay Mythry, D. Jackuline Moni "A 76dB 828nV/√Hz Low Noise Bio Signal OTA for Neural Signal Recording Applications" International Journal of Engineering & Technology, Vol. 7 (3.3) (2018). [Scopus Indexed]

[4]. Sarin Vijay Mythry, D. Jackuline Moni "High Gain Low Noise Bulk Driven Folded Cascode Ota For Electroencephalograph Activity", International Journal of Pure and Applied Mathematics, Volume 120, No. 6, July 2018. [Scopus Indexed]

[5]. Sarin Vijay Mythry, D. Jackuline Moni "A 21nV/√Hz 73 dB Folded Cascode OTA for Electroencephalograph Activity", Communications in Computer and Information Science book series (CCIS, volume 837), 416-424. [Springer & Scopus Indexed]

[6]. Sarin Vijay Mythry, D. Jackuline Moni "High flat gain low noise neural signal recording amplifier", IEEE International Conference on Signal Processing and Communication [ICSPC 2017], Coimbatore, Tamil Nadu. [IEEE & Scopus Indexed]

[7]. Sarin Vijay Mythry, D. Jackuline Moni "A 21nV/√Hz 73 dB Folded Cascode OTA for Electroencephalograph Activity", International Conference on Soft Computing Systems (ICSCS 2018) during April 19-20, 2018. [Springer & Scopus Indexed]

[8]. Sarin Vijay Mythry, D. Jackuline Moni "Low Power High Flat Gain Amplifier for Recording Low and High Frequency Signals" International Journal of Science, Engineering and Technology, 2017.

[9]. Sarin Vijay Mythry, D. Jackuline Moni. "Low Power High Flat Gain Amplifier for Recording Low and High Frequency Signals" National Conference on Communication and Image Processing [NCCIP 2017].

[10]. Sarin Vijay Mythry et al "Design of Low Power Operational Transconductance Amplifier for Biomedical Applications" International Journal of Applied Control, Electrical and Electronics Engineering (IJACEEE) Vol.3.No.1/2, May 2015.

[11]. Sarin Vijay Mythry et al "Design and Analysis of High Gain CMOS Telescopic OTA in 180nm Technology for Biomedical and RF Applications" International Journal of Microelectronics Engineering (IJME) Vol.1, No.1, May 2015.

[12]. Sarin Vijay Mythry et al "Design of Low Power and High Frequency Radio Modulations and Telecommunication Systems" International Journal of Modelling, Simulation and Applications (IJMSA) Vol.1, No.1, July 2015.

[13]. Sarin Vijay "Low-Power Clock Sharing Double – Edge Triggered Flip-Flop". National Conference at Karunya University, Coimbatore, March, 2009.

[14]. Sarin Vijay "Clock Shared Low Power Double – Edge Triggered Flip-Flop". National Conference at COEIT, Jalgaon, Maharashtra, March, 2009.

REPUTED JOURNAL REVIEWER:

1. **IEEE TRANSACTIONS ON VLSI**
2. **IEEE ACCESS**
3. **COGENT ENGINEERING [TAYLOR & FRANCIS]**

RESEARCH INTERESTS:

1. Low Power VLSI
2. Biomedical Electronics
3. Digital IC Design
4. CAD for VLSI & CAD Tools

MEMBERSHIPS IN ASSOCIATION OF ENGINEERS:

- **IAENG**
- **IETE**

NPTEL SWAYAM PROGRAM:

- **Analog Circuits**
- **CMOS Digital VLSI Design**
- **Integrated Circuits, Mosfets, OP-Amps and their Applications**
- **Neural Science for Engineers.**
- **Python for Data Science**
- **Data Science for Engineers**
- **User-Centric Computing for Human-Computer Interaction**

EXPERIENCE:

- ☐ Presently working as Assistant Professor at Walchand Institute of Technology in E&TC Department.
- ➔ Guest Faculty at **SR University**, Warangal from June 2020 to December 2020.
- ➔ Worked as Research Associate and Intern at **CDAC Research center**, Hyderabad during January 2017 to October 2019 **(INDUSTRY EXPERIENCE).**
- ➔ Worked as Faculty in ECE & EEE department of Christu Jyothi Institute of Science and Technology, Jangaon, Telangana State from September 2014 to December 2016. Overall, I have 11.5 years of experience as a part of teaching and research.
- ➔ From February 2013, I am working as Research Scholar in Karunya University, Coimbatore, India on Low Noise Amplifiers for RF Ultra Wide Band and Biomedical Applications. I have an experience of four plus years in research field.
- ➔ Four years (4) as Assistant Professor in Guru Nanak Dev Engineering College, Bidar, Karnataka from August 2009 to December 2012.
- ➔ Conducted a National Workshop on Trends in VLSI Design & Mentor Graphics Tool **"TVDM'11"** in 2011 as co-ordinator. And have conducted **six National Level workshops** and attended nearly ten workshops and conferences on VLSI area.
- ➔ Guided final year students in coming up with their engineering projects on VLSI domain and helped to get **placement in core industries and their clients like Mentor Graphics, Ascentronics, Tevatron, Matchwell Technologies and Solutions etc.**
- ➔ Have got the experience in handling final year laboratories for their practical benefits.

PERSONAL PROFILE:

Name : M.SARIN VIJAY
Father's Name : M.Solomon
Mother's Name : M.VijayaKumari
D.O.B : 29-05-1985
Sex : Male
Marital Status : Married
Languages Known : English, Telugu, Kannada, Hindi and Tamil.

ADDRESS

PERMANENT

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Telangana State-502001.

PRESENT

M.SARIN VIJAY
Door no: 7-7-201/1
MahaLaxmi Nagar,
Chilukawada, Jagitial,
Telangana State-505327.

DECLARATION

I Pledge and pronounce that all the above furnished details are true to the best of my Knowledge.

Place :
Date :

Yours' truly
SARIN VIJAY MYTHRY