**Characterizing Charge Plasma-based Junctionless TFETs for Biosensors**

***Rajendra Kumar1\*, Akanksha Singh2***

1Department of Physics, Rama University, Kanpur-209217, India

2Electronics & Communication Department,Rama University, Kanpur-209217, India

*\*Corresponding Author, E-mail:*[*rajendrab25@gmail.com*](mailto:rajendrab25@gmail.com)

**Abstract—**The aim of this chapter is to talk about the analysis and characterization of Charge Plasma-based Junctionless TFETs for Biosensor devices. Despite the device's obvious advantages, the steep doping profile associated with classic Tunneling Field Effect Transistor (TFET) poses significant production issues. By providing a constant doping profile across the device, junctionless TFETs (JL-TFETs) considerably reduce the problem. In this study, we looked at a variety of device variables that affect device performance, such as gate insulator dielectric constant, gate insulator thickness, silicon body thickness, doping level, and P-gate and source work function. The investigation is centered on the parameters that influence sub threshold swing (SS), on-current to off-current ratio (Ion/Ioff), and threshold voltage (VT). The effect of various parameters on on-current (Ion) has also been investigated. These have allowed us to identify how parameter adjustment can lead to peak device performance.

***Keywords*:** Junctionless TFET, Sub threshold Swing, Work Function, Threshold Voltage, Non-local Band-to-Band Tunneling Model

**I. INTRODUCTION**

Field-effect transistors (FETs) have improved sensitivity, reliability, and compactness to improve biosensing technology. Due to their ultra-low power consumption and improved performance, junctionless tunneling FETs (TFETs) are promising.

The benefits of charge plasma-based junctionless devices are used to study the complex relationship between TFETs and biosensing. This study analyzes their electrical characteristics and sensitivity to maximize biosensor development.

Years of aggressive scaling of MOSFETs have resulted in an unfavourable increase in short channel effects, leakage current, and subthreshold swing for MOSFETs is also limited to 60 mV/dec [1]. As a result, extensive research is being performed to hunt for alternative technologies. The tunneling field effect transistor (TFET) is one of the most promising of these devices [2-4]. Because of the band-to-band tunnelling mechanism, TFETs have significantly smaller sub threshold swing than MOSFETs [5-7]. Furthermore, because of its huge tunnelling barrier in the off state, TFET has lower leakage current, ultra-low power dissipation, and very low off current. However, the fabrication of TFETs requires a high doping concentration and an asymmetric doping structure, which presents a considerable challenge to our research's existing fabrication technology [8]. However, such issues can be addressed with junctionless TFETs (JL-TFETs), in which a uniformly doped silicon device can achieve a P-I-N doping configuration utilising the charge-plasma concept [9-10].

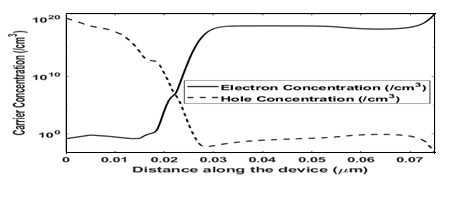
**II.JUNCTIONLESSTFET DEVICE STRUCTURE**

A junctionless TFET (JL-TFET) is built in the same way as a standard TFET, but instead of p-i-n doping, a uniformly doped silicon body wafer is used. The p-i-n doping profile in the structure is built via work function engineering. As a result, the cost and complexity of doping throughout the production process can be minimized. Fig. 1 illustrates a schematic view of the JL-TFET. The work functions of the source, gate, and drain electrodes were set to 5.40 eV, 4.20 eV, and 3.90 eV, respectively. Furthermore, the P-Gate (gate above the source area) has a work function of 5.40 eV. The silicon body thickness is 10 nm, the dielectric thickness is 3 nm, and the dielectric constant of the gate insulator is 7. There is 1018cm3 of uniform n-type doping in the silicon body. The above-mentioned parameters are held constant while the parameter of interest is changed. It should be mentioned that a 5 nm high-spacer (k =21) is used. The P-gate measures 20 nm in length, whereas the control gate measures 25 nm in length. In this inquiry, VDS has been set to 1 V for all simulation types.



**Fig. 1.** Device Schematic of JL-TFET.

The formation of a p-i-n area can be seen in the ON state, as depicted in Fig. 2. The optimal selection of work function has a considerable impact on JL-TFET performance [12].



**Fig. 2.** A Graph of carrier concentration (*κ*=16) in the ON state.

Fig. 3 shows a transfer curve of a JL-TFET (=16 for gate insulator) with VGS swept from 0 V to 2 V.



**Fig. 3.** Transfer curve of a JL-TFET.

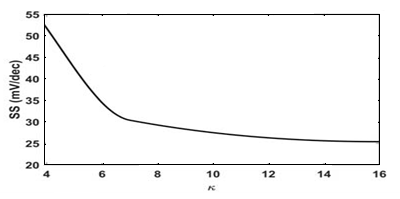
**III. METHODOLOGY**

To simulate the device, a non-local band-to-band tunnelling model is used, which takes into account the tunnelling process's inherent non-locality. Furthermore, Fermi-Dirac statistics, concentration-dependent mobility, bandgap narrowing, trap-assisted tunnelling (TAT), Auger recombination, and Shockley-Read-Hall rearrangement are used (SRH). Fermi Statistics is used to calculate the intrinsic carrier concentrations required to assess SRH recombination. The Newton method is used to solve numerical issues.

**IV. SIMULATION RESULT**

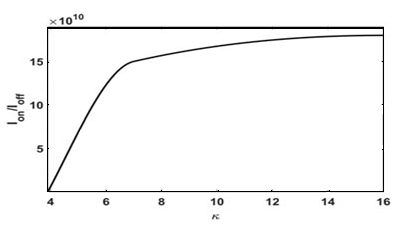
***A. Effects of κ on JL-TFET***

We changed the dielectric constant of the gate insulator as follows to observe the effect on JL-TFET: SiO2 (=3.9), Si3N4 (= 7), and Y2O3 (= 16). We discovered that using a larger dielectric constant reduces the sub threshold swing, as seen in Fig. 4. These findings are consistent with that of Ghosh et al. and Bal et al. in their studies published in [10] and [11-12], respectively. These advantages are due to the higher gate coupling ability of high-insulators. Ion is more controlled because to its greater gate controllability.



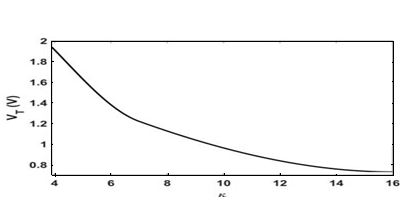
**Fig. 4**. SS improves as *κ* increases.

Improves notably when high-*κ* gate dielectric is used resulting in improvement of I*ON*/I*OFF* ratio as illustrated in Fig. 5.



**Fig. 5.** I*ON*/I*OFF* increases significantly with the increase of *κ*.

As seen in Fig. 6, increasing the threshold voltage enhances the performance. In the constant current technique, 109A/m is used as the current to determine the threshold voltage, despite the considerable variance in current with respect to changes in some parameters. As is also seen fromour study that using high-*κ* materials could lead to improved performance. This is consistent with the study in [13].



**Fig. 6.** V*T* and *κ* have negative correlation.

**B. Effects of doping level in JL-TFET**

Table I illustrates how the doping level is changed to investigate the effect of doping level. As the quantity of doping increases, an increasing or decreasing pattern of Ion and VT may be observed. Even if increased doping levels result in little improvements, it should be noted that the effects of doping levels are not as relevant as some other parameters. The overall low on-current values owe to the comparably low value of and high tins used during parametric variation*.*

TABLE IEFFECTS OF DOPING LEVEL ON I*on* AND V*T*

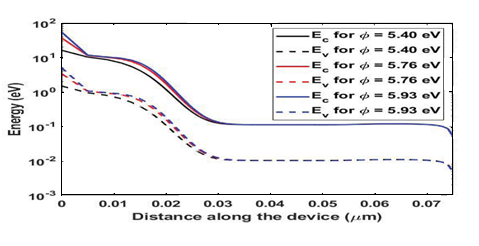
|  |  |  |
| --- | --- | --- |
| **Doping level (/cm3)** | **I*on* (*A/μm*)** | ***VT* (V)** |
| 1017 | 4*.*61 *×* 10*−*8 | 1*.*30 |
| 1018 | 4*.*63 *×* 10*−*8 | 1.29 |
| 1019 | 5.65 *×* 10*−*8 | 1.24 |
| 1020 | 6*.*61 *×* 10*−*8 | 1.22 |

***C. Effects of P-Gate and Source work function on JL-TFET***

We've seen the effects of work function on device performance. Table II shows how on-current and threshold voltage fluctuate when the work function changes. As shown in Fig. 7, the ion rises with increasing energy barrier width, resulting in increased tunneling current. Furthermore, the threshold voltage is inversely proportional to the work function.

**TABLE II EFFECTS OF P-GATE AND SOURCE WORK FUNCTION ON I*on* AND V*T* .**

|  |  |  |
| --- | --- | --- |
| ***φ* (eV)** | **I*on* (*A/μm*)** | ***VT* (V)** |
| 5*.*50 | 4*.*61 *×* 10*−*8 | 1.22 |
| 5.60 | 3*.*25 *×* 10*−*8 | 0.98 |
| 5.70 | 1*.*22 *×* 10*−*8 | 0.66 |



**Fig. 7.** Band diagram for different work function values.

**V. CONCLUSION**

JL-TFET is one of the most famous TFET modifications because it can overcome the constraints frequently found in normal TFET manufacture. We discovered that employing a high-gate dielectric improved the performance of the JLTFET device in this study. Tin decrease improves SS, Ion/Ioff, and VT. Furthermore, when the thickness of the silicon body decreases, Ion increases and VT decreases. Furthermore, a rise in doping level can lead to improvements in Ion and VT, though the effects are subtle. Gate work function engineering has a significant impact on both Ion and VT. Our findings can aid in the process of selecting parameters for best device performance in JL-TFETs.

**REFERENCES**

1. S. Gupta, K. Nigam, S. Pandey, D. Sharma, and P. N. Kondekar, “Effect of interface trap charges on performance variation of heterogeneousgate dielectric junctionless-tfet,” *IEEE Transactions on Electron Devices*, vol. 64, no. 11, pp. 4731–4737, 2017.
2. J. Madan and R. Chaujar, “Gate drain underlapped-pnin-gaa-tfet for comprehensively upgraded analog/rf performance,” *Superlattices andMicrostructures*, vol. 102, pp. 17–26, 2017.
3. R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, “Cmoscompatible vertical-silicon-nanowire gate-all-around p-type tunnelingfets with \_ 50-mv/decade subthreshold swing,” *IEEE Electron Device Letters*, vol. 32, no. 11, pp. 1504–1506, 2011.
4. J. K. Mamidala, R. Vishnoi, and P. Pandey, *Tunnel field-effect transistors(TFET): modelling and simulation*. John Wiley & Sons, 2016.
5. J. H. Kim, S. Kim, and B.-G. Park, “Double-gate tfet with vertical channel sandwiched by lightly doped si,” *IEEE Transactions on ElectronDevices*, vol. 66, no. 4, pp. 1656–1661, 2019.
6. A. Alian, Y. Mols, C. Bordallo, D. Verreck, A. Verhulst, A. Vandooren, R. Rooyackers, P. Agopian, J. Martino, A. Thean *et al.*, “Ingaas tunnel fet with sub-nanometer eot and sub-60 mv/dec sub-threshold swing at room temperature,” *Applied Physics Letters*, vol. 109, no. 24, p. 243502, 2016.
7. J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, “Band-to-band tunneling in carbon nanotube field-effect transistors,” *Physical reviewletters*, vol. 93, no. 19, p. 196805, 2004.
8. Kaity, S. Singh, and P. Kondekar, “Silicon-on-nothing electrostatically doped junctionless tunnel field effect transistor (son-ed-jltfet): A short channel effect resilient design,” Silicon, pp. 1–15, 2020.
9. P. Bal, B. Ghosh, P. Mondal, M. Akram, and B. M. M. Tripathi, “Dual material gate junctionless tunnel field effect transistor,” Journal of Computational Electronics, vol. 13, no. 1, pp. 230–234, 2014.
10. Ghosh and M. W. Akram, “Junctionless tunnel field effect transistor,” IEEE electron device letters, vol. 34, no. 5, pp. 584–586, 2013.
11. K. Dash, P. Saha, and S. K. Sarkar, “Analytical modeling of asymmetric hetero-dielectric engineered dual-material dg-tfet,” Journalof Computational Electronics, vol. 17, no. 1, pp. 181–191, 2018.
12. S. Kumar, K. S. Singh, K. Nigam, V. A. Tikkiwal, and B. V. Chandan, “Dual-material dual-oxide double-gate tfet for improvement in dc characteristics, analog/rf and linearity performance,” Applied Physics A, vol. 125, no. 5, p. 353, 2019.
13. M. A. Raushan, N. Alam, M. W. Akram, and M. J. Siddiqui, “Impact of asymmetric dual-k spacers on tunnel field effect transistors,” Journal of Computational Electronics, vol. 17, no. 2, pp. 756–765, 2018.