Current Mirror and Current Limiter Based High Performance Voltage Level Shifter

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***Abstract***-The paper presents a high-performance voltage level shifter design based on a current mirror and current limiter circuit. The proposed circuit can shift a low voltage level signal to a high voltage level signal with low power consumption and high-speed operation. The current mirror circuit is used to generate a reference current, which is then compared with the input current using a current limiter cir- cuit to control the output voltage. The proposed design achieves a wide voltage range and a high output impedance, making it suitable for various applications, including low- power and high-speed applications. Simulation results demonstrate the effectiveness of the proposed design in terms of low power consumption, high speed, and excellent performance. The proposed circuit can be implemented in various technology nodes, making it a promising solution for future integrated circuits.

**Keywords-**Current limiter, Delay, IoT application, Level shifter, Power consumption.

**I.INTRODUCTION**

A voltage level shifter is an essential component in elec- tronic circuits that enables the translation of signals between different voltage domains. The current mirror and current limiter based voltage level shifter is a high-performance solution that provides accurate and reliable voltage transla- tion with minimal power consumption.

The current mirror is a circuit that produces an output current that is proportional to the input current. In a current mirror-based voltage level shifter, the input voltage is con- verted to a current using a simple transconductance amplifi- er, and this current is mirrored to the output stage to gener- ate the desired output voltage. The current limiter, on the other hand, is a circuit that limits the maximum current that can flow through a device. In a current limiter-based voltage level shifter, the input current is first limited using a current limiter, and then the limited current is mirrored to the output stage to produce the desired output voltage.

The combination of these two techniques in a voltage level shifter results in a circuit that is capable of translating signals between voltage domains with high accuracy and low power consumption. This makes it an ideal solution for applications where signal integrity and power efficiency are critical, such as in portable devices, data acquisition sys- tems, and sensor networks.

# EXISTING SYSTEM

The most common current-limiters are implemented to have a voltage drop from too high for their low-voltage sup- ply rails. The design with a lower voltage drop is the better fit. In many cases where the supply voltages need the inter- nal current-limiters, they are usually built using current sen- sors, control circuits, and pass transistors. The current sen- sors are the simple low-value resistors built up with MOS transistors.

The circuit current limiters MN1 and MN2 MOS transistors weaken the current contention of the pull-up network. When the voltage input VIN is at voltage low to voltage high tran- sition, MOS transistor MN5 makes pull-down ON.

This will invert the output by MN8-MP4 inverter with full swing output voltage VOUT. At VIN high to low voltage transition the possible short circuit current at the output in- verter can increase. To avoid another pair of current limiters MN3-MN4 have introduced.

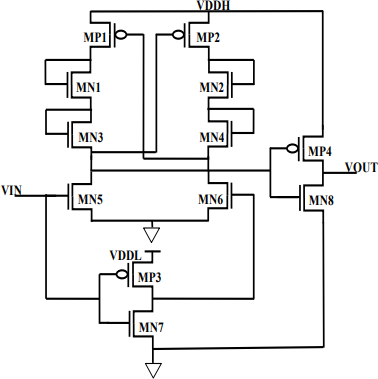


Fig. 1. DCVS Level Shifter

VIN is logic ‘1’, i.e.as low as 0.15V, then MOS transistor MN5 turns ON and VDDL inverter MP3-MN7 produces a strong logic ‘0’, will make MN6 OFF.

When MN6 is ON the driving inverter MP4-MN8 produces the strong logic ‘1’, i.e. 1.25V through the pull-up MP4 ON.

When the voltage swing is low in the main conversion stage and the current is limited through the current limiters MN1- MN2 and MN3-MN4 the better power consumption and delay could be able to achieve.

# Disadvantages

1. High delay
2. High power consumption

# PROPOSED METHOD

The proposed level shifter circuit consists of two voltage levels one is low voltage level (VDDL) another high voltage level (VDDH), here we are able to achieve the better power consumption and delay when compared to existing voltage level shifter.

The proposed level shifter is designed by using current mirror and current limiter circuit. Current limiter circuit is used to limit the current flow and avoid the short circuit path.

The simple current mirror circuit is designed by connecting the drain terminal of PMOS or NMOS to the gate terminal of the same transistor.

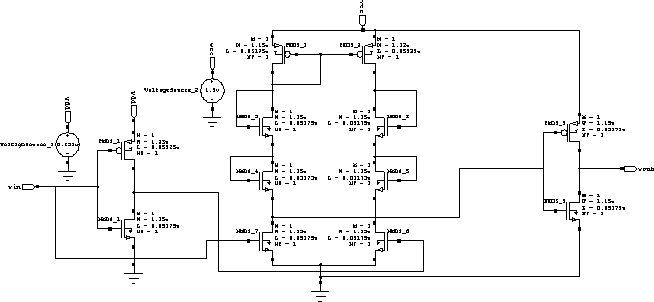


Fig 2.Proposed Method

The current in one transistor will exactly mirror that of the second, assuming that both transistors are accurately matched. It will provide the constant current.

Here input supply voltage in the range of 0.29v to 0.4 v can able to achieve up to the high voltage level 1.5v.

When VIN is logic ‘1’, then NM7 transistor is on NM6 is off .

Here the current limiter is avoid the short circuit path and power consumption of the level shifter and delay can be achieved.

# LITERATURE SURVEY

The LS “An Ultra-Low Voltage-Level Shifter Using Re- vised Wilson Current Mirror for Fast and Energy-Efficient Wide-Range Voltage Conversion from Sub-Threshold to I/O Voltage” is a Wilson current mirror model. Wilson current mirror involves an input controlled diode and feedback con- trol makes LS accomplishes small propagation delay and less power dissipation for wide voltage conversion from below threshold to I/O range. It additionally utilizes “Mixed-device and Inverses narrow width device” sizing to improve the overall delay and power.

**Summary:** From this article, sizing is used to improve the overall delay and power.

The LS entitled “Low-Power Level Shifter for Multi Supply Voltage Designs is a modified DCVSL architecture” is the DCVSL model. In this paper novel, low-power LS for vigorous voltage shifting from the near or sub-threshold to the above threshold voltage is proposed. The design exploits design strategies to limit energy and static power. Because of these highlights, the proposed LS exhibit lower static power and energy.

**Summary:** From this article, Level shifter exhibit lower static power and energy.

# IV.RESULTS AND DISCUSSION

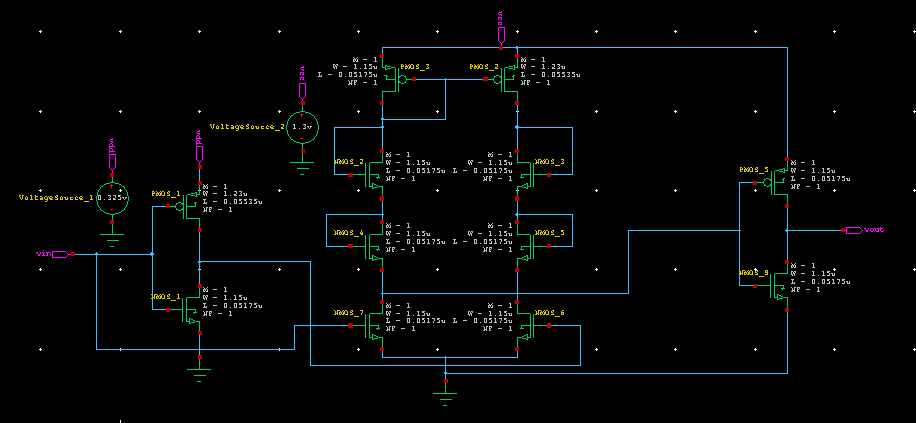


Fig 3.Schematic of proposed Schmitt trigger

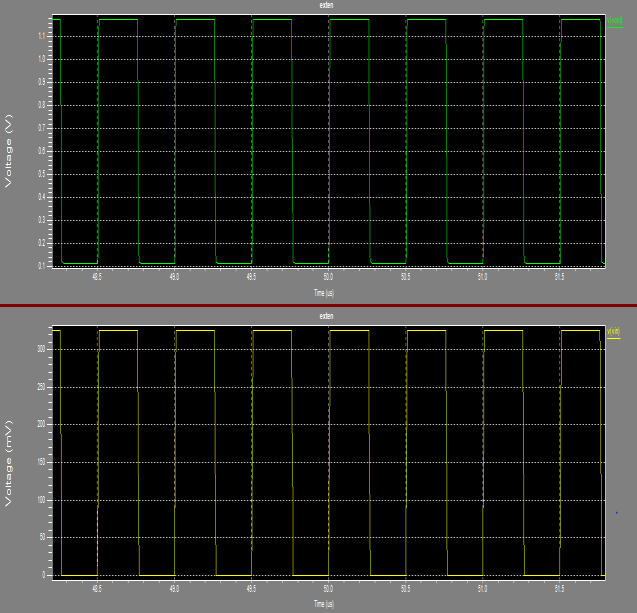


Fig 4.Simulated output of differential pair of the proposed Schmitt trigger

|  |  |  |
| --- | --- | --- |
| PARAMETER | EXISTING METHOD | PROPOSED METHOD |
| Power | 6.2315 | 5.991 |
| Dealy | 2.9526 | 0.5466 |
| Area | 12 | 12 |

Table 1:Comparision Between Existing and Proposed Level Shifter

# CONCLUSION:

The proposed current mirror and current limiter based high performance voltage level shifter circuit is designed by using 45nm CMOS technology to perform the voltage level shifting from 0.3V to 1.4V. The results prove that the pro- posed circuit comfortably shifts at low power consumption. The proposed design can be as robust because of the wide conversion range as well as meeting all the requirements of IOT requirements.

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