**Modeling and Simulation of H6 Topology using Single Phase Transformerless Grid Connected Photovoltaic System**

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**ABSTRACT**

This paper proposes a new technology of solar energy system, which is gaining immense popularity due to the increase of importance to research on alternative sources of energy over depletion of the conventional fossil fuels all around the world. The systems which are being developed extract energy from the sun in the most efficient manner and suit them for the available loads without affecting their performance. In this paper, the design and control issues associated with the development of a 1.8 kW prototype single-phase grid-connected photovoltaic system of multilevel cascaded inverter are discussed. For the system current controller, a ramp time zero average current error control system algorithm combined with an optimized cyclic switching concept sequence is suggested. Simulation results of Grid tie inverter have been presented to demonstrate the suitability of the total control method. The Simulation results exhibit improved performance under the presence of harmonics and the studied system is modeled and simulated in the MATLAB / Simulink.

**Keywords−**Maximum power point tracking, Interleaved Flyback converter, H6 topology, SCR ­­­­Bridge.

# INTRODUCTION

PV inverter is becoming popular due to unsolvable centralized maximum power point tracking (MPPT) mismatching issue during partial shading situations [1-4]. Module integrated converter system is thus proposed to overcome the issue [5]. With each panel is optimized with its own MPP Tracker (MPPT), the resolution is higher. Thus the system achieves higher efficiency. Such systems are called as AC Modules integrated converter (MIC) or inverters. Several inverter topologies are introduced for PV applications. Transformerless ones came up for its small size, but they have issue with the panel’s Parasitic capacitor [6]. Also a DC-link capacitor is required in between the inverter and the converter. Inability to scale its output voltage into several times higher also makes the topologies impractical to serve in countries with high grid voltage. To overcome the voltage boosting issue, cascading isolated converter to an inverter is proposed [7]. It then connects to a low frequency unfolding inverter to flip the polarity making the output as sinusoidal waveform. This way the DC-link capacitor is reduced to only the one next to the panel. Additionally, aside from the MPPT, the only control task is on the DC-DC converter to shape its output as desired. Flyback converter has its dynamic similar to that of buck boost converter, but it utilizes a transformer to provide a large voltage step-up ratio and galvanic isolation. Due to the existence of a non-minimum phase (NMP) zero [8] and system dynamic issue [9] in CCM, the topology has instead been designed to operate in DCM. Thus mixture of operation is suggested for such systems [10, 11].The control problem for CCM, however, has recently been overcome by using a simple analog controller [8, 12] for the current controller. Another method is sampling the output from grid side filter instead [9], making it possible to control the system using digital controller. Even though the system is designed under CCM operation, it also works very well in DCM during grid voltage polarity shifting period [12]. These designs knowingly improve the topology efficiency, but distortions in the output current are also there [8, 9, 12]. This paper offers a topology for interleaved flyback inverter sharing two common switches and grid-side filter with other converters from different panels. To do so, primary current control scheme is needed [8].

**II.HIGHER EFFICIENCY FOR BOOST CONVERTER**

For these single stage grid tied inverters, either a transformer is used for boosting the input voltage or the input voltage will be required to be higher than the peak of the grid voltage. But this requirement is not good for PV applications because the solar panel’s characteristics changes all the time. The energy storage needs to be at the front of a single stage inverter and it is mainly implemented by electrolytic capacitors. Although the electrolytic capacitors have limited lifetime, it can still be used by applying minimum voltage and current ripple to prolong its lifetime. Because the end of its life doesn’t mean it failed, the electrolytic capacitor can work maximum longer than its estimated lifetime. As the capacitance also has an impact on Maximum power point tracking (MPPT) efficiency, the maximum capacitance leads to higher MPPT efficiency. Later on, a boost-buck converter based inverter is proposed. This system can operate in either boost or buck mode; thus, a wide input voltage range or high efficiency can be achieved. Then the system analysis of its middle capacitor and CCM/DCM operation condition is presented. Since the common-mode voltage in the flyback inverter is equal to the grid voltage, it changes at line frequency. Its leakage current is very small even at an extreme case.

**III.SYSTEM STRUCTURE OF SINGLE STAGE GRID CONNECTED INVERTER**

A single-stage controller solar inverter system block diagram is shown in Figure 1. It tracks the array of maximum power and outputs in AC current supplying the utility grid [3]. The inverter system consists of a solar-array source, bulk input array filter, capacitor CBULK, line-filter, DC/DC converter, 50/60Hz switching bridge, output filter and a system controller design. The system controller can be decomposed into six basic control sub-systems namely (1) maximum power point tracking (MPPT), (2) solar-system array voltage regulation, (3) converter output average-current regulation, (4) DC/AC switching bridge inverter, (5) compensated current supplying reference generator and (6) utility over-voltage protection.

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**Figure 1 Single Stage Maximum Power Tracking Solar Inverter**

The application of solar-array voltage and solar-array current as the feedback signals, the MPPT control sub-system continuously updates the set-point voltage reference. The set-point voltage reference commands the solar-array voltage regulation sub-system (or voltage regulation error amplifier) to produce the error voltage drive signal for regulation of the solar-array voltage, at the corresponding level. Upon reaching a steady state operation, it is controlled to swing back and forth around the peak-power array system voltage with acceptable AC ripple voltage of the frequency at twice as much the utility frequency. The signal is sufficiently band-limited to have negligible AC ripple voltage, especially at twice the utility frequency despite the presence of the converter power stage to deliver properly the output current of the rectified sinusoidal wave shape. Subsequently, the DC/AC switching bridge inverter sub-system provides switching control at the utility frequency of 50/60Hz switching bridge that converts into an AC current in synchronization with the AC utility voltage and system delivers to the utility grid the in-phase AC current with low total-harmonics distortion [4]. When an over-voltage is detected from the rectified utility voltage, the over-voltage protection sub-system further reduces the error voltage drive signal through an active pull-down transistor Q. Under this condition, either the absolute average of regulated voltage at a predetermined level of the power converter is shut down while the absolute average already exceeds the predetermined level [5-7].



Figure 2 Full-Bridge Phase-Shift DC/DC Converter and Full-Bridge Unfolding Circuit

A full-bridge unfolding circuit is connected to the inverter for converting the rectified sinusoid current into sinusoid current, which will be switched in 50/60Hz frequency. Without high-frequency switching, the unfolding circuit has much higher efficiency than a high-frequency PWM conventional inverter.



Figure 3 Block Diagram of a Solar-Based Inverter System

From Figure 3, the solar-based inverter system will include five separate parts namely full-bridge phase-shift DC/DC converter, unfolding circuit and conditioning board, DSP controller board and load monitor. The conditioning board senses the voltage and current of the solar system array and sends these signals to the DSP controller board. The DSP controller will regulate the solar system array working under the maximum power point and drive the full-bridge phase-shift DC/DC converter and unfolding the circuit to deliver the sinusoid current to the load or utility grid.

**IV.INTERLEAVED ACTIVE CLAMP FLYBACK DESIGN.**

The interleaved flyback converter was selected as a single stage topology that can boost the low PV panel voltages (20-45 V DC) to a rectified AC output and both sides are provided a galvanic isolation from the PV panel and the grid. Flyback converters are generally used in low power system and step-down applications. The system less than a couple maximum watts have a grid side low output current. A forward converter can also step up the PV panel voltage and provide galvanic isolation. When comparing the operation of two topologies, the flyback converter requires fewer components as there is no freewheeling diode required on the output side or the need for an output inductor; For this purpose only, the interleaved clamp flyback topology is selected and then the created system energy is also stored in the clamping capacitors. If correctly implemented, the active clamp circuit also provides Zero Voltage drop switching on the flyback MOSFET, which reduces the switching losses and improves the overall efficiency.



Figure 4 Active clamp flyback converter

The DC-AC inverter is a standard single-phase full bridge based on IGBTs with ultrafast co pack diodes, as depicted in Figure 4. The connection to the grid is realized by means of current control performed in DQ rotating reference frame. An LCL filter is placed between the bridge and the grid in order to reduce the current harmonics generated by the unipolar sinusoidal pulse-width modulation (USPWM) at 17 HHz. L filters or LC filters may also be chosen for the application, but in the first case large values of inductance are required to perform good high frequency noise damping and large currents through the capacitor may arise in the second case together with high voltage harmonics. LCL filters show good performance in terms of current harmonic reduction but they may lead to instability of the control loop in the presence of large grid impedance.

**V PROPOSED BUCK-BOOST BASED ON PV INVERTER**

A boost-buck type of circuit dc-dc converter is proposed as the first stage with regulated output inductor current. A full-bridge converter unfolding circuit with 50 or 60 Hz line frequency is applied to the dc-ac stage, which will unfolding clamp the rectified sinusoid current regulated by the dc-ac stage into a pure sinusoidal current, as shown in Figure 5. Since the circuit runs either in boost or buck mode, its first stage can be very efficient if the low conduction voltage drop switching power MOSFET and ultra-fast reverse recovery diode are used. For the second stage, due to the unfolding circuit only operates at the no loss line frequency and switches at zero voltage and current, the switching loss can be rejected. The only loss is due to the conduction voltage drop, which can be minimized with the use of low drop power devices, such as thyristor or slow-speed IGBT. In this version, IGBT is used in the unfolding circuit because it can be easily turned on and off with gating control. Since only the boost dc-dc converter or buck dc-dc converter operates within a high frequency switching, the efficiency of proposed system is improved all the time. In addition, reliability can be greatly enhanced because there is only one high operating frequency power processing stage in this complete PCS. Then the analysis of middle capacitor and CCM/DCM operation condition is also presented. Figure 6.show the diagram of Buck-boost based PV inverter.



Figure 5 Buck-boost operation mode



Figure 6 Buck-boost based PV inverter

**VI BOUNDARY MODE ANALYSIS**

As already discussed, during the buck mode, the input current can be treated as the input filter’s inductor’s current, whose ripple is reduced from the filtering effect. Similarly, during the boost mode, the output current can be treated as output circuit filters and inductor’s current, whose ripple is also much mitigated. Due to this dual filter effect, the DCM mode operates very rarely in the proposed circuit. In fact, the circuit is always running in continuous current mode (CCM) for input current in buck mode and output current in boost mode. This operation also indicates that discontinuous current mode (DCM) or boundary mode can happen only in output current in buck mode and input current in boost mode. Then it can be analyzed as a normal buck and boost converter. The boundary condition can be derived based on the input current ripple for boost mode and output current ripple for buck mode as shown in Figure 7 and 8.

  **Figure 7 Boundary power condition for Input current Figure 8 Boundary power condition for output**

 with different input voltage current with different input voltage

**VII LEAKAGE CURRENT ANALYSIS**

It is inferred that the capacitance between the point of contact and a single PV module always lies in the range between 100–400 pF. The capacitance value depends on weather conditions, and in the worst case as rainy days, the capacitance can be as high as 80 nF/KW. Because of no isolation between the input and output without a transformer, the transformerless grid tied inverter needs to consider the leakage current issue as shown in Figure. 9.



Figure 9 Leakage current in grid tied inverter system

Because of this safety issue, the leakage current should be as small as possible for transformerless inverter. Many literatures analyzed the leakage current in transformerless grid-connected inverter. For the proposed topology, the negative terminal of solar modules is set as the reference point, and the middle points of the bridge legs are set as phase and neutral for the output terminals. Since grid voltage is not constant but sinusoidal with 60 Hz, there is a small line frequency leakage current in the proposed inverter. For a 2.5 kW system, the capacitance between the PV modules and the ground CPV would as high as 200 nF.

**VIII CONTROL OF THE BOOST –BUCK MODE PV INVERTER**

During buck mode, inductor current can be treated as normal buck converter’s output inductor current which can be easily controlled. However, it is critical to control inductor current in boost mode because the control target in this mode is output circuit filters’ inductor current. Thus, the compensator for boost mode needs to be designed first and then applied it to buck mode. In practice, if the boost mode is stable and well controlled, buck mode will be stable and well controlled. The loop gains of boost mode at different operating points are shown in Figures 10 and 11. It clearly shows that the RHP zero and double pole make 2700 phase delay, which makes it difficult to be compensated. Thus, the compensated crossover frequency needs to be before double-pole’s frequency of the boost mode and ensured that the peak Q value is lower than 0 dB. In order to have a compensator that is good for every operation point, the compensator design is system based on the worst conditions, which is defined as a condition with highest Qpk and the earliest phase drop. In our case, worst condition happens when input voltage is the lowest defined value 200 V and output voltage is the peak voltage of the grid 340 V.



Figure 10 Analog control for smooth



Figure 11 Digital control for smooth

In order to achieve smooth waveform in transition between boost to buck modes, an offset of the saw tooth carrier right on the top of the buck mode PWM modulator needs to be applied to boost mode as shown in Figure 12.



Figure 12 Block diagram of the buck boost single phase voltage source inverter

The maximum power point tracking power can be implemented as an outer loop with lower bandwidth control, providing the magnitude of the output current reference for smooth transition between buck and boost modes respectively.

## **Grid-Tie Converter Controller**

To transfer the energy to the grid, the following controller algorithm must be realized in this system:

1. Phase-locked loop (PLL) controller logic is used to synchronize with the grid voltage, which can provide a reference system phase to the current controller.

2. Grid-tie current controller can ensure the output current is a sine wave signal and trace the current reference to balance the input power and the output power.

3. Maximum power point tracking (MPPT) is used to track the panel into a maximum power output stage.

4. The phase error detection detect the phase error between the reference and the sine wave out. This detection is done in 1ms task A0. The PLL controller and the closed loop controller operations are executed in 1ms task A0. The Sine generator systems generate the sine wave according to the frequency and sample time which is done in the ISR. The equation (1) and (2) represent load sharing transfer function as

*Ipv1(s) = Gd, ipv1(s) Xd(s)*  (1)

*Ipv2(s) = Gd, ipv2(s) Xd(s)* (2)

Let the error between the currents be equal to ΔI.

The equation (3) represents a load sharing current error as

*Ipv1(s) = Ipv2(s) = ΔI = (Gd, ipv1(s) – Gd, ipv2(s)) X d(s)* (3)

The objective is to make both the currents the same (i.e. make *Ipv1* as *Ipv1(s) – ΔI/2* and *Ipv2* as *Ipv2(s) + Δ I/2*) by including correction factors of *±Δd.*

The equations (4) and (5) of load sharing the correction factor are

*Ipv1(s)-ΔI/2 = Gd, ipv1(s) X (d(s) - Δd(s))* (4)

*Ipv2(s) + ΔI/2 = Gd,ipv2(s) X (d(s) + Δd(s))* (5)

The equation (6) of a load sharing current,

*ΔI = (Gd, ipv2-Gd, ipv1) d(s) + (Gd, ipv2+Gd ipv1) Δd(s)* (6)

Assuming *Gdipv2 ≈ Gdipv1 ≈Gdipv*

*ΔI(s) = 2Gdipv(s) Δd(s)*



Figure 13 current control loop

Using the system of PI controller, the controller operating frequency is 22 KHz. The open loop bandwidth must be set to 1 to 2 KHz. Figure 13 indicates that the feedback of the closed loop must be the primary side current ip, but in the real system it is the curve middle point current when Q1 is turned on in the real system. If the converter is working in a continuous mode, the relationship between the system of primary feedback and the secondary average current is to get a sine wave output current. The secondary average current must be a sine wave signal. Therefore, it is necessary to modify the output feedback current to the following model in figure 14.



 Figure 14 modified current loop

**IX SIMULATION MODEL AND RESULTS**

1. **GRID AND PLL SIMULATION**

The PLL is integral to the operation of the inverter in that DC/AC conversion is managed in synchronism with the AC line. All state management is synchronized to the line. All inversion-related control operations are synchronized to the line. The only item that is not directly synchronized to the line (although it could be) is the ripple cancellation control algorithm. The PLL is operated slightly differently than that of other PLLs for this design. Simulation model of proposed System and Interleaved Flyback Inductor Simulation Sytem are shown in figures 15 and figure 16.



**Figure 15. Simulation model of proposed System**



**Figure 16. Interleaved Flyback Inductor Simulation Sytem**

A line cycle is divided into 1024 slices, or 512 slices per half-sine and the number of slices does not change. However, the distance between each slice is allowed to change. One key advantage is that the sine reference information is always the same. Figure 17 and 18 represents Average flyback input currents and Current error.



Figure 17 Average flyback input currents



Figure 18 Current error

The load sharing local load and grid to control loop constantly monitors the error between the input currents of the converters and will minimize this error. It also dynamically adjusts the duty ratio of each of the converters by the addition/subtraction of a small common correction factor value depending on the sign of the error.

A combined feed-forward and feedback system can improve the system performance of the control system to a large extent, whenever there is a major measurable disturbance. In an ideal situation, gain of the feed-forward compensator will completely reject the measured disturbance signal better than the compensator acting alone. The main role of the feed-forward compensator in the solar inverter system is to provide the steady state duty ratio D(t), to the sharing system, thereby allowing the compensated value to the error system. The feed-forward network will help the compensator to reject the disturbances caused by fluctuations in both the solar panel input voltage and the output voltage of the grid. The load resistance has been included in the term, Rf, next one for a filter inductor and DCR is in series to the load resistance in the AC-equivalent circuit. From the open-loop bode plot, it can be observed that both gain margin and phase margin of the system are low and thus, the system inherently has a poor relative stability. Additionally, it is mainly observed that the switching frequency ripples attenuation needs improvement and that the system gain at the required system operating frequency (100/120 Hz) is very low. Grid current and current reference and Grid voltage are shown in figures 19 and 20.



Figure 19 Grid current and current reference



Figure 20 Grid voltage



 Figure 21 Ripple control result



 Figure 22 DC/AC controlled output current

Therefore, the MPPT loop and the current control loop appears as a unity gain system with zero or minimal phase error. The current loop modulates the converter current into a rectified signal as a sine wave output. Ripple control result and DC/AC controlled output current are shown in figures 21 and 22.The MOSFET full-bridge unfolds this rectified current into an alternating current to be delivered to the grid. The current loop bandwidth can be improved through the use of a gain feed forward compensator. The steady-state duty cycle can be dynamically computed using the measured PV panel voltage and AC grid voltage. While the feed-forward compensator supplies the steady-state modulation, the current control loop takes into account dynamic variations and modulates the controlled current accordingly. The following sections discuss the transfer function calculation and mathematical modeling of the solar inverter system to obtain the transfer functions of output to control input and control output to disturbance inputs of the system.

**CONCLUSION**

A new system control approach for a solar-based inverter that tracks the maximum available power and produces a near unity power factor is presented. It is inferred that the new approach produces excellent signal-to-noise ratio for the feedback signals, ensuring reliable and robust Maximum power point tracking (MPPT) while tightly regulating the sinusoidal waveform of AC current supplied to the utility grid with the unity power factor. While employing a feed-forward compensation technique coupled with one stage of the DC/DC power conversion, the proposed inverter system is simplified when compared to conventional inverter deigns. This dissertation suggested a single stage boost-buck converter based high efficiency grid-tied PV inverter. Based on its unique operation mode, the proper control method is proposed for smooth mode transition. Based on the similar concept, three other inverters with both step-up and step-down functions are proposed. In addition, three advanced control methods are also proposed. Based on the operation mode concept, many topologies can be proposed. If any inverter is working based on buck converter’s concept, it can be integrated with boost part. As a result, the new inverter won’t have the limitation on its input voltage, which means the input voltage doesn’t need to be higher than the peak of the output ac voltage. In this way, the input voltage range could be widened and the topology has lower switching losses and improve the overall system efficiency. High efficiency is achieved by implementing a novel interleaved active-clamp flyback topology with to Zero Voltage Switching (ZVS).

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