Switching Analysis for Three-Level Action of

Two-Level Three-Phase Dual VSI

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*Abstract* – The most common way for a variable voltage and frequency supply is by inverters. Multi-level converters have gotten a lot of attention when it comes to multi-level inverter networks. Power electronics technology has advanced so far that high safety voltages with lower harmonics can now be achieved. One reason for harmonics in output voltage may be switching inside the inverters. Pulse Width Modulation (PWM) techniques were developed for Two-Level (2-L) 3-phase voltage source inverters (VSI), however, SVPWM is the much popular approach because of easier digital implementation and improved dc bus use. Comparison of the two switching patterns of a dual inverter system with three phases for a Three-Level (3-L) operation is shown in this article. The performance was evaluated in the output phasing voltages on the basis of total harmonic distortion. For 3-L operation and simulation results, a complete Simulink model for three-phases VSI provides validation of this comparison.

Keywords— Dual 2-L VSI, Space vector pulse width modulation (SVPWM), 3-L voltage source inverter, Total harmonic distortion.

# Introduction

In today's world, the most common power electronic system for converting DC to AC power at the desired frequency and output voltage is the inverter. They have divided into two types: 2-L inverters and multi-level inverters. Lots of research has been done on multi-level inverters and 2-L multi-phase inverters in the last decade [1-2]. Multilevel inverters have many benefits over 2-L inverters, including the ability to implement processes at various voltage levels, and less harmonic distortion. Multilevel inverters are using in a variety of applications, including static VAR offset, active power filter, rolling mills, etc. [3-4]. A detailed discussion about multi-phase multi-level inverters electric drives has done in [5]. 3-L working using 2-L dual inverter has presented in the literature using space vector modulation strategy [6], even the 3-L inverter configuration has presented using 2-L inverters connected in cascading in [7]. Decouple based space decomposition scheme has presented for a 3-L inverter in [8] and a carrier-based approche for a dual 2-L inverter in [9]. An open-end winding (OEW) three-phase induction motor has discussed with isolating transformer in [10] and switching strategy for 3-L dual inverter has presented in [11] based on space vector PWM. Multi-phase multi-level inverter based on four 3-phase 2-L inverters has presented in [12]. For the 5-phase open-end drive, the PWM scheme for the multi-level operation has presented in [13]. Multilevel multiphase inverters benefit from the use of SVPWM techniques. The standard SVPWM strategies have an analogous carrier-based pulse width modulation (CBPWM) counter-part that generates similar effects, for both multilevel (three-phase) inverters and (2-L) multiphase inverters. Multilevel multiphase SVPWM technique has presented in the study, which combines phase disposition pulse width modulation with an effective zero-sequence injection scheme [14-16]. Dual 2-L inverters and multi-level inverters are having the same number of switching devices, but additional capacitors and diodes are required in multi-level inverters for voltage balancing operation. While using a dual-level inverter for multi-level operation, no additional diodes and capacitors are required (17-20). This paper analyzes 3-L switching operation using 2-L dual three-phase VSI using SVPWM for two different switching patterns. Both switching patterns are producing the same results along with the same total harmonic distortion.

# Three-phase dual voltage source inverter

Figure 1 displays the circuit diagram for the 2-L 3-phase dual voltage source inverter. The output of both the inverter is connected to an OEW and both inverters are powered by two isolated DC voltage sources.

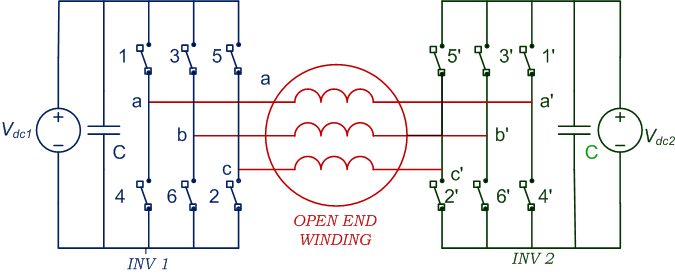


Fig. 1. Circuit configuration for three-phase dual inverter system

Fig. 1 shows that each three-phase inverter has six switches, but only three are independent because the behavior of two power switching devices on the same leg is complimentary. When these three states of switching are coupled, there are eight possible space voltage vectors. Six of the eight vectors (states 1-6) create non-zero output voltage, whilst the other two (states 0 and 7) produce null output voltage and also are referred to as zero voltage vectors. As illustrated in fig. 2, the space vectors create a hexagon with six unique sectors, every of which spans 600. A set of three vectors (two active and one zero) may be selected in space vector PWM to synthesis the required voltage in each switching period and provide a reference vector at any point in time.



Fig. 2. Representation of all the switching states

Three-phase input voltages are

 (1)

Voltage vector in space is defined as

 (2)

where and. The space vector is a representation of all 3-phase quantities at the same time. In contrast to the phasors, it is a complex variable that is a function of time. To generate the PWM signals, the PWM time intervals for each sector are

(3)

(4)

(5)

Where,

*k* = sector number (*k* = 0, 1…..6 for athree-phase),

= voltage vector length.

= reference Vector (maximum value is

Ts *=* sampling Time,

T0 = time of application for zero vectors and

α = angle between & V1.

The reliance of time spans T1, T2 and T0 are just on the peak value and angle α of the reference vector.

# 3-L operation using 2-L three-phase dual VSI

There are two three-phase voltage source inverters, each of which produces two reference voltage vectors, Vref and Vref '. During sampling time, these two reference voltages are used to add three voltage vectors closest to the reference vector to generate an average voltage vector. Reference voltages, Vref and Vref ' circulate in a hexagon with six sectors (I to VI). During 3-L operation, both systems have 12 active vectors of voltages for inverters (V1 to V6) for inverter-1 and (V1' to V6') for inverter-2, as well as two null voltage vectors (V0 & V0') at the origin, as illustrated in fig. 3a & 3b. Inverter functioning necessitates lowering switching states to shrink switching losses and total harmonic distortion. Tables 1 and 2 show the sequence pattern in all six sectors for both Vref and Vref' reference voltage vectors to recognize a 3-L operation with a dual 2-L VSI.

Table 1. Switching pattern-1 for 3-L operation

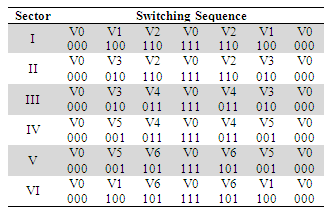


Table 2. Switching pattern-2 for 3-L operation

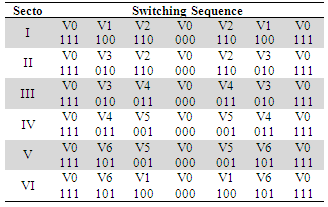


Figure 4(a) for switching pattern-1 shows the overall switching sequence and output voltages of the two inverters for both reference voltages Vref & Vref' indicated in sectors I & IV. Simplicity was achieved by using blue for inverter-1 and green for inverter-2. The voltage vectors for inverter-1 and inverter-2 are analyzed using the voltage vectors V0, V1, V2, and V0', V4', and V5', respectively. In sampling time Ts, Figure 4(a) illustrates the Vab and Va'b' line voltages for both inverters.

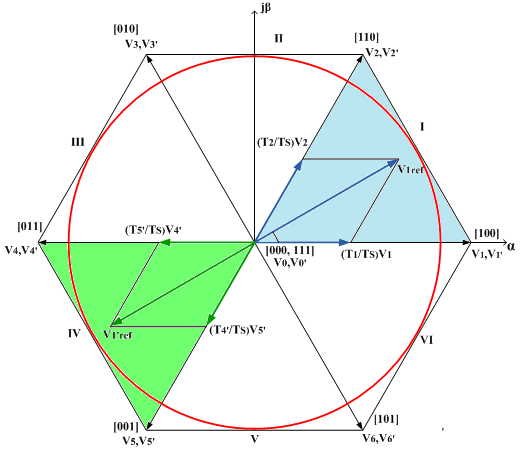


Fig. 3a Space vector diagram with switching sequence pattern 1

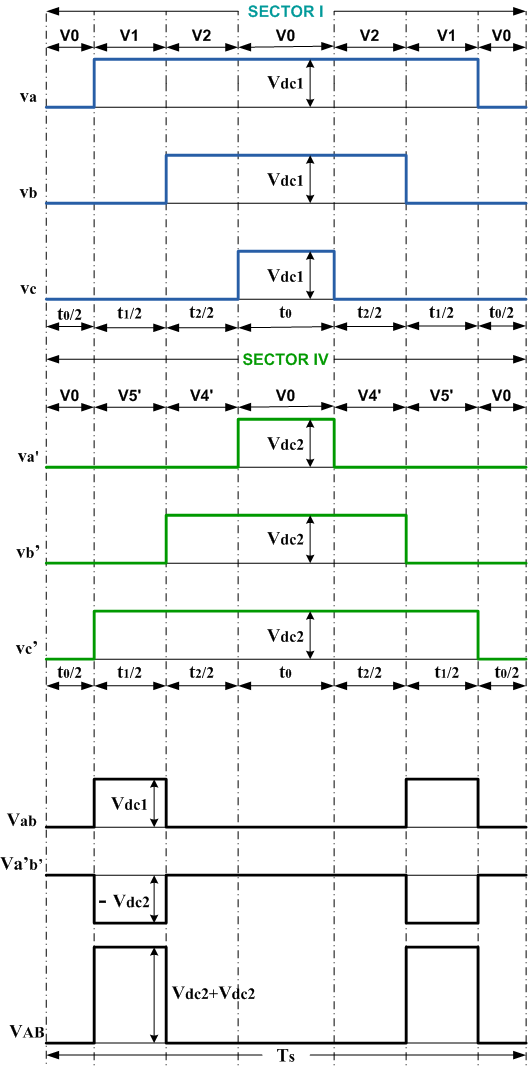


Fig. 4a. Switching pattern 1 3-L operation

Because the time period between zero states is adequate, switching losses can be minimized when employing dual 2-L VSI to generate 3-L output as indicated in switching pattern-2. There is no need to change when the reference vector goes from one sector to another. As a result, in order to reduce switching losses, the reference vector goes in the opposite direction of the preceding sector, and the time of active vectors in even and odd sectors will change.

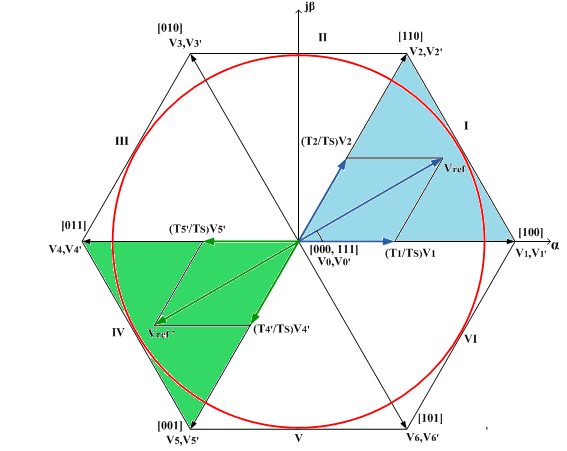


Fig. 3b Space vector diagram with switching sequence pattern 2

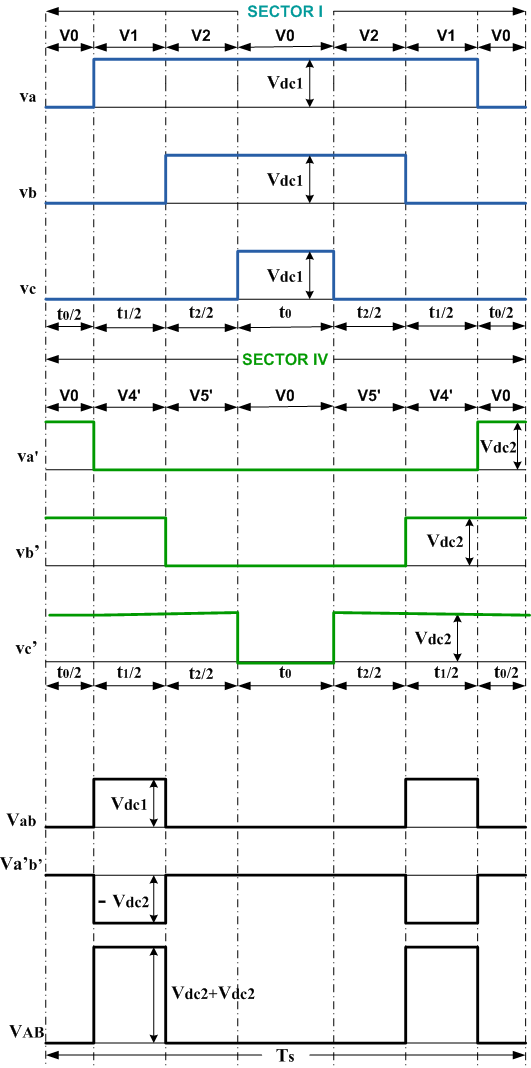
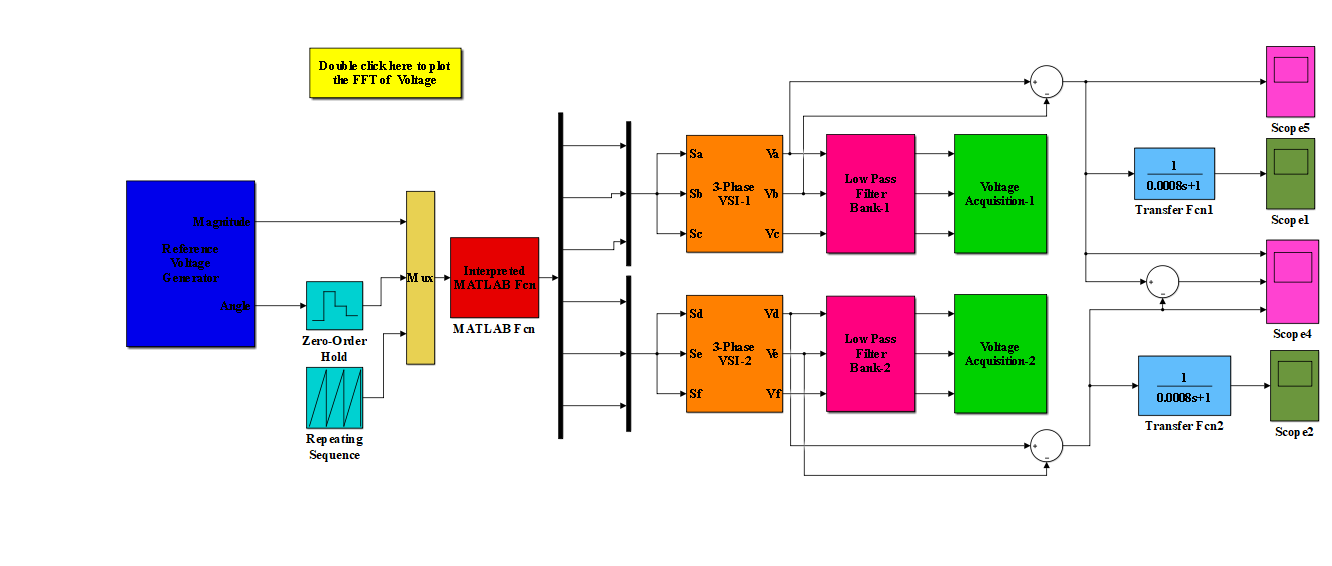


Fig. 4b. Switching pattern 2 for 3-L operation

# Simulation results & discussion

A Simulink model of a 3-phase VSI using several blocks is shown in Figure 5. This section details a step-by-step MATLAB / SIMULINK model for a three-phase VSIusing SVPWM. The function block takes a 3-phase sinusoidal voltage as input and outputs the angle and magnitude of reference. To calculate switching time and generate the switching pattern for every semiconductor switch, the Matlab code is used. This block's inputs are the magnitude, corresponding angle of reference, and repeating sequence. The phase voltages are produced by a three-phase VSI block. It uses a first-order filter having 0.8 ms time constant to filter the data. The output is kept in the workspace by the voltage acquisition block. Simulation results have shown in Figure 7 – Figure 11. Table 3 compares the simulations results at various switching frequencies based on fundamental component, total harmonic distortion, and weighted total harmonic distortion. The bar chart presentation is shown in Figure 6 at various frequencies.

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**Fig. 5.** Simulation model for dual inverter configuration

Table 3.Comparison of fundamental part, THD and WTHD for different switching frequencies

|  |  |  |  |
| --- | --- | --- | --- |
| **Switching Frequency** | **Fundamental Component**  **(peak)** | **THD** | **WTHD** |
| 3kHz | 0.1750 | 0.94% | 0.75% |
| 4kHz | 0.2305 | 0.57% | 0.19% |
| 5kHz | 0.2879 | 4.74% | 5.38% |
| 6kHz | 0.2904 | 8.01% | 8.38% |
| 7kHz | 0.2849 | 11.62% | 12.16% |

Figure 7 depicts the phase voltages of inverter-1 and 2 without filter, which are identical in both switching schemes, while fig. 8 depicts the filtered voltages of phase. The results of simulation are in per unit value, with the dc voltage set to one and the switching frequency set to 5 kHz with a fundamental frequency of 50 Hz, as simulation parameter. Fig. 9 illustrates a single fundamental voltage, with a magnitude of 0.2036 p.u. rms (0.2879 peak) at a 50Hz frequency, along with the harmonic spectrum of the inverter for the output phase 'a' voltage. The output voltage is near the sinusoidal and has a total harmonic distortion of 4.74% of the fundamental voltage.

# Conclusion

This paper presents a comparison of two switching schemes for 3-L operation using 2-L dual VSI. As compared to multi-level inverters with complex circuitry, both schemes have proven to be very useful in reducing switching losses and harmonic content. Both schemes are easy, feasible, and dependable to implement. The simulation findings will be tested in future experiments.

Fig. 6. Bar chart representation for simple reference and comprehension

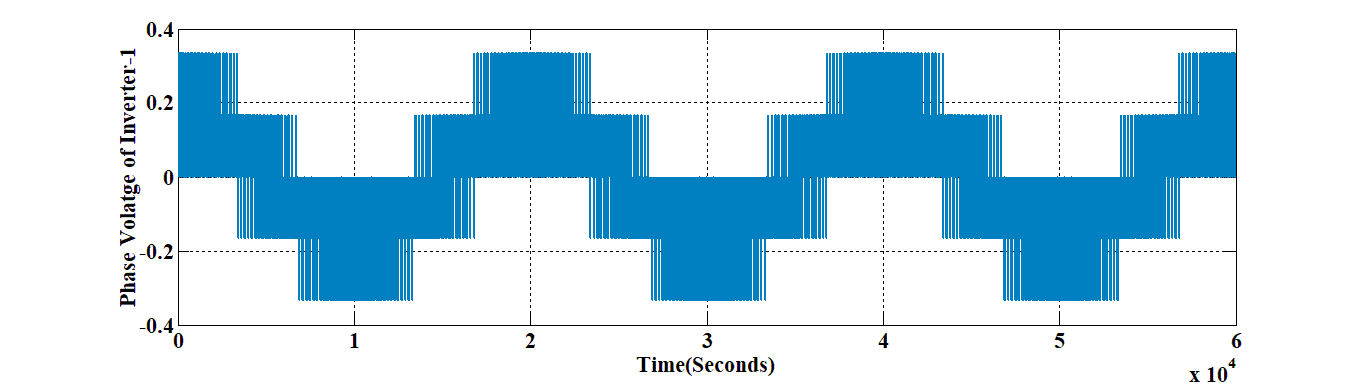


Fig. 7a. Inverter-1 phase voltage

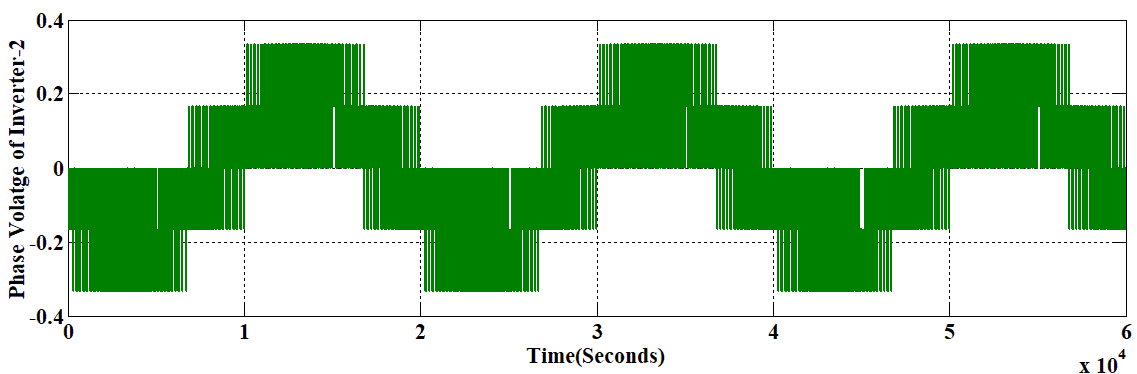


Fig. 7. Inverter-2 phase voltage

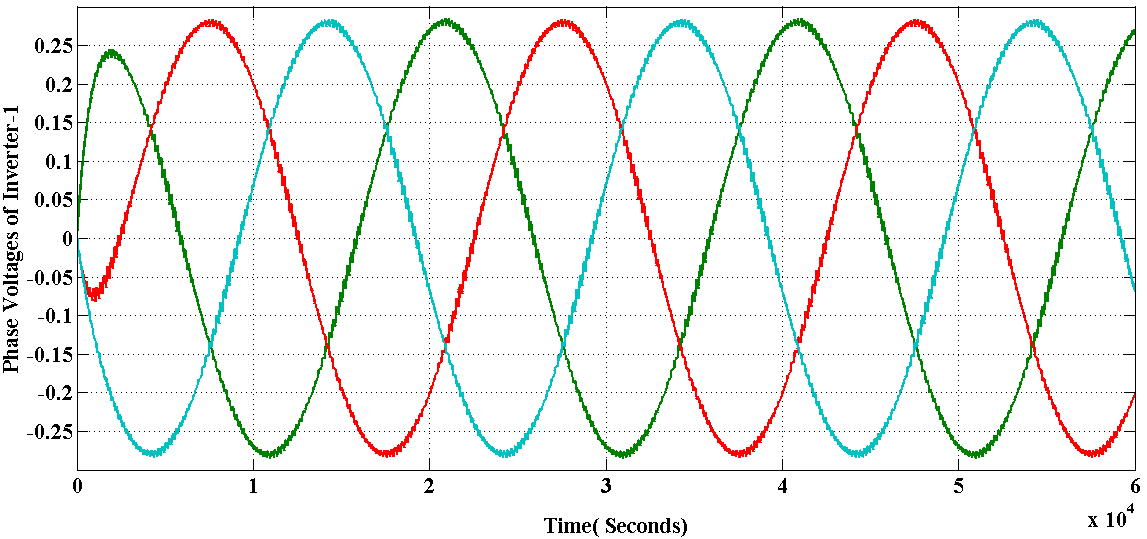
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Fig. 8a. Filtered phase voltages of inverter-1

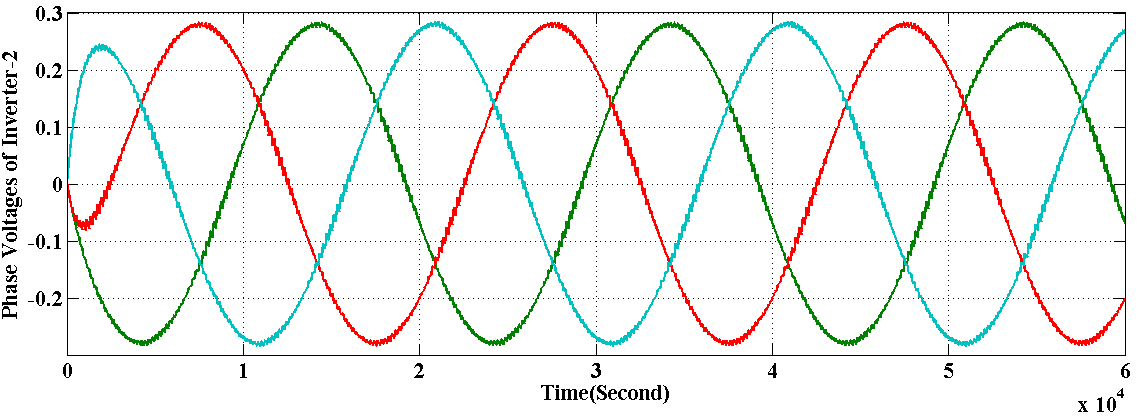
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Fig. 8b. Filtered phase voltages of inverter-2

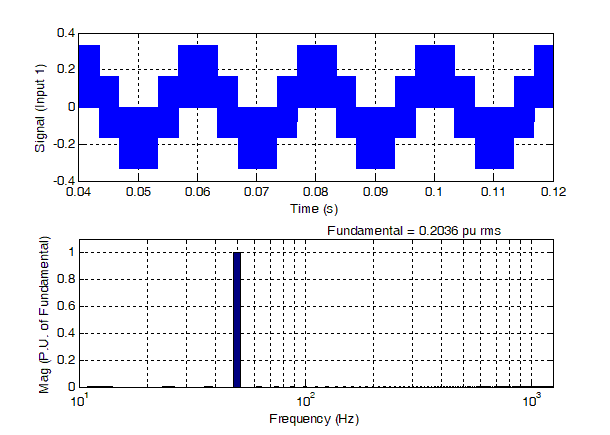
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Fig. 9. Harmonic representation in inverter output voltage for phase ‘a’

##### References

1. J. S. Lai and F. Z. Peng, “Multilevel converters - A new breed of power converters”, *IEEE Transactions Industrial Application*, vol. 32, pp. 509-517, 1996.
2. S. Bernet, S. Kouro, J. O. Pontt, J. Rodriguez and B. Wu, “Multi-level voltage-source-converters topologies for industrial medium-voltage drives”, *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930-2945, 2007.
3. D. Casadei, G. Grandi, A. Lega and C. Rossi, “Multilevel operation and input power balancing for a dual 2-L inverter with insulated DC sources”, *IEEE Transactions Industrial Application,* vol. 44, no. 6, pp. 1815-1824, 2008.
4. J. Lai and F. Peng, “Multilevel inverters: A survey of topologies, controls and applications”, *IEEE Transactions on industrial electronics*, vol. 49, no. 4, pp. 724-738, 2002.
5. E. Levi, “Multiphase electric machines for variable-speed applications”, *IEEE Transactions on Ind. Electronics*, vol. 55, no. 5, pp. 1893-1909, 2008.
6. Y. Kumsuwan and W, Srirattanawichaikul, “A space vector modulation strategy for 3-L operation based on dual 2-L voltage source inverters”, IEEE International Power Electronics Conference (IPEC-Hiroshima 2014-ECCE ASIA), Hiroshima, Japan, 2014.
7. K. Gopakumar and V. T. Somasekhar, “3-L Inverter configuration cascading two 2-L inverters” *IEEE Proc-Electronic Power Appl.* vol. 150, no. 3, pp. 245 – 254, 2003.
8. J. Chen,  Y. Hu, Y. Wang and Z. Wang, “Decoupled Vector Space Decomposition Based Space Vector Modulation for Dual Three-Phase 3-L Motor Drives”, *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10683 – 10697, 2018.
9. R. Baranwal, K. Basu and N. Mohan, “ Dual two level inverter carrier SVPWM with zero common mode voltage” IEEE International Conference on Power Electronics, Drives and Energy Systems, Bengaluru, India, 2012.
10. S. L. Arevalo, S. Chowdhury, C. Gerada and P. Wheeler, “A dual inverter for an OEW induction motor drive without an isolation transformer, Conference Proceeding. IEEE Applied Power Electronics Conf. and Exposition, IEEE-APEC'15, Charlotte, NC, USA, 2015.
11. S. Srinivas and V. T. Somasekhar, “Space-vector-based PWM switching strategies for a 3-L dual-inverter-fed OEW induction motor drive and their comparative evaluation”, *IET Electonics Power Appl*., vol. 2, no. 1, pp. 19–31, 2008.
12. G. Grandi, A. Tani, P. S. Kumar and D. Ostojic, “Multi-phase multi-level ac motor drive based on four three-phase 2-L inverters”, International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM 2010), pp. 1768 – 1775, 2010.
13. E. Levi, I. N. W. Satiawan, N. Bodo and M. Jones, “A space-vector modulation scheme for multi-level OEW five-phase drives”, *IEEE Transactions on Energy Conversion*., vol. 27, no. 1, pp. 1-11, 2012.
14. Ó. López, J. Álvarez, A.G. Yepes, F. Baneira, D. P. Estévez, F. D. Freijedo, J. D. Gandoy “Carrier-Based PWM Equivalent to Multilevel Multiphase Space Vector PWM Techniques”, *IEEE Transactions on Industrial Electronics,* vol. 67, no. 7, July 2020.
15. S. K. Gupta & Md. Arif Khan, “[Space Vector Modulation Strategy for Three Level Operation of Five-Phase 2-L Dual VSISystem](https://www.edas.info/showPaper.php?m=1570664151)”,*17th IEEE India Council International Conference (INDICON-2020),* NSUT,New Delhi, 11-13 Dec, 2020.
16. S. K. Gupta, O. Singh Md. A. Khan & D. K. Chauhan, “Pulse Width Modulation Technique for Multitier Operation of Five-Phase Twin Voltage Source Inverters”, *Journal Européen des Systèmes Automatisés*, Vol. 54, No. 2, pp. 371-379, April, 2021.
17. S. K. Gupta, O. Singh & M. A. Khan, “Three Level Operation for Seven-Phase Dual Voltage Source Inverter, proceeding of *International Conference on Smart Technologies for Power and Renewable Energy (PECon 2021),* Federal Institute of Science And Technology (FISAT), Mookkannnoor, Kerala, February 1 - 3, 2021.
18. S. K. Gupta, “THD Analysis of Twin 2-L 5-Phase Inverter System for Multi-Level Performance using Two Switching Schemes”, *IEEE Delhi Section International Conference on Electrical, Electronics and Computer Engineering (DELCON-2022)*, NSUT, New Delhi, 11-13 Feb., 2022.
19. S. K. Gupta and O. Singh, “Analysis of Dual Two-Level Converters for Multilevel Performance”, Multilevel Converters: Advances and Applications (MCAA2023), Wiley-Scrivener, Scrivener Publisher, 2023.