Switching Study of Twin Two-Level Seven Phase Voltage Source Inverter System for

Multi-Level Outcome

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*Abstract* – Various industrial high-power applications, such as electric boats, hybrid cars, and ship propulsion, use multilevel inverters. However, as the number of levels rises, so does the complexity of multilevel inverters, which has certain drawbacks. Some of the drawbacks of multilevel inverters can be solved by a dual two-level inverter system. Double two-level (2-L) 3-phase inverter topologies with an OEW that is fed from both ends with a VSI are utilized for rolling mills, electric ship propulsion, VSD applications, as well as HEVs/EVs applications. The author of this article uses two different switching of space vector pulse width modulation techniques to suggest a multi-level outcome for a twin two-level seven-phase voltage source inverter system. This kind of research has never been done before. The total harmonic distortion (THD) and basic component performance of the system were investigated using simulation findings. To back up the conclusions, simulation data have been presented.

Keywords—Space vector PWM, dual 2-L seven phase Inverter, Multiphase inverter, Overall harmonic distortion.

# Introduction

In the last few decades, a great deal of study has been done on variable speed drives. This is the result of combining an inverter with a motor. Two-level voltage source inverters are utilized to power the motor drives. To obtain the regulated output, a suitable modulation technique must be utilized. A three-phase motor and inverter is a viable choice due to the widespread availability of three-phase power. However, the degree of flexibility in a three-phase drive is limited.

Due to advancements in power electronics devices, a multiphase machine can surpass the limits of three-phase machines. Polyphase machines improve system dependability and provide a number of advantages over three-phase machines, which are detailed in [1-2]. To offer polyphase machines with improved options for obtaining broad power ratings utilizing current limiting components, polyphase inverters are required. To regulate output voltages, many pulse width modulation techniques are available in the literature, but the most popular is the PWM approach based on space vectors. The five-phase inverter [3-6] and the nine-phase inverter [7], where the n-leg, n-phase inverter has been generalized, have each received a comprehensive description of this system. The modified space vector pulse width modulation approach for seven-phase has been presented with all vectors in the d-q plane for the reference space voltage vector [8-9].

The author of this work gives an overview of multi-level operation for a two-level seven-phase dual voltage source inverter device. In the first portion, the seven-phase system was modelled and then a simulation study was presented for review. Two switching strategies for the system and simulation results were discussed in the next sections. In terms of total harmonic distortion, both switching patterns provide the same results.

# Twin two-level seven-phase voltage source inverter

The multi-tier functioning of a seven-phase two-tier dual voltage source inverter is investigated. The inputs of both inverters are connected to an isolated dc supply, and the outputs of both inverters are saved in workspace for analysis. Each inverter has seven legs, each of which has two semiconductor devices such as IGBTs or MOSFETs. As a consequence, each inverter has fourteen semiconductors. Using the typical space vector PWM scheme concept, each inverter has a total of 138 switching voltage vectors, with 126 active and 2 null vectors.

# Applications of twin two-level inverter system: a review

Twin two-level inverter reduces the limitations of multi-level inverter topologies. Hence it is required first to find out the various application areas of it. The author summarize various applications of Twin two-level inverter system.

As a solution to the voltage limit problem, two inverters are employed, with the objective of sharing the required voltage. The secondary inverter only handles the reactive voltage component, which climbs fast in high-speed operation. As a result, the secondary inverter doesn't need to be powered by another source. Only a capacitor bank is required for the secondary inverter. In 2004, instead of a permanent synchronous machine, the author experimented with an induction machine [10]. In 2005, a hybrid car with twin three phase inverters coupled to an open end-winding AC motor and energy storage was presented [11].In 2005, an SVPWM switching approach for dual inverter fed open-end winding induction motor drive was suggested to minimize the CMV suited for applications requiring repeated starting and low speeds [12]. V. Oleschuk et al. discuss the results of using an unique synchronized space-vector pulse width modulation (PWM) for control of twin inverter-fed traction motor drives in 2007, using two insulated dc sources with an open-end winding induction motor [13]. Lega A proposed a dual two-level inverter scheme in 2007 to improve the efficiency of the system in various applications such as fishing boats and ships, as well as in applications such as automotive traction systems and land traction systems because it overcomes the max power limit of switching devices and increases the power [14]. A dual two-level inverter configuration based generation system for series hybrid power train & naval ship propulsion systems is proposed in 2008 [15].

A dual-seven-level inverter configuration for an open-end winding IM drive for fault tolerant applications is proposed in 2009[16]. Levi E proposed open-end winding variable speed drives with dual-polyphase inverter supply for electric and hybrid electric vehicles in 2010[17]. A charging technique to charge the secondary battery in dual inverter system is presented for application like electric vehicles as topology used in such application which have one charger for primary battery only [18]. The author proposed SVPWM method in dual two-level five phase inverter system for battery powered applications [19-22].

# Svpwm in twin two tier seven phase VSI [21]

The dwell duration of each voltage vector utilized in the synthesis process is measured in seconds. Each inverter generates an average voltage vector by combining the three vectors closest to the reference voltage vector in the sampling time using two reference voltage vectors provided by Vref & Vref. For inverters, there are 252 active voltage vectors (V1 to V126) for INV 1 and (V1' to V126') for INV 2. The synthesis process' null voltage vectors (V0& V0') are at origin. During the synthesis process, the key mathematical equation required for both the adjacent active vector for time and the active vector for space is

(1)

(2)

(3)

Where symbol denotes their usual meaning. Table 1 shows the switching order for multi-level operation. For inverter operations, switching losses and switching states, as well as overall harmonic distortion, must be minimized. Table I and II represent the switching order of the two-level dual VSI for a multi-level outcome. In scheme-01, voltage vector of sector I and VIII combined produce the same outcome as in scheme-02 produced by that of sector I and XII.

Figure 1 shows the switching waveforms for both Vref and Vref' reference values using scheme 01 of the twin inverter system's output voltage, while Fig. 2 shows the switching waveforms using scheme 02 for the same. In scheme 1, the sectors I and VIII are used to produce the average voltage vector, whereas in scheme 2, the sectors I and XII are used to generate the average voltage vector. Using the voltage vectors V0, V1, V2, V0', V8', and V9'(scheme 1) and V0, V1, V2, V0', V12', and V13'(scheme 2) for easy comprehension, the switching wave form and order is depicted in blue for inverter-1 and green for inverter-2.

As shown in Figure 1, the switching order is V0, V2, V1, V0' and V0', V1, V2, V0. To begin and end, we utilise the switching order [0 0 0 0 0 0 0] so that no switching is required while going from one sector to the next. We move in the opposite direction in the following sector to ensure minimum switching losses when migrating from one vector to another. As a consequence, T1 and T2 values will be switched for adjacent sectors, i.e., T1 and T2 values will remain the same in sectors 1, 3, 5, 7, 9, 11, 13 but will be swapped in sectors 2, 4, 6, 8, 10, 12, 14.

# Simulation study

A multi-level operating simulation model of a two-level seven-phase dual voltage source inverter was constructed for analysis, and the simulation results were presented for principle validation. Figure 3 depicts the fundamental Matlab/Simulink model. The Simulink model employs several blocks from the planned seven-phase dual VSI for multilevel operation.

The switching pattern and application time for switching vectors were generated with the help of the MATLAB code. Figure 4 illustrates the produced output phase voltages for INV 1 and INV 2. The output phase voltages pass through the first-order filter, which produces filtered phase voltages with a time constant of 0.8ms. For all seven phases, Figure 5 depicts the filtered phase voltages for INV 1 & INV 2. During the simulation of synthesis phase, the settings were unity dc-link voltage and 50 Hz fundamental frequency.

Figure 6 shows the harmonic spectrum for phase voltage 'a' at 5k switching frequencies. The harmonic spectrums clearly demonstrate that it has a fundamental component magnitude at 50 Hz. At 50 Hz, the fundamental component is 0. 433758 p.u. (0.613333812 peak), and THD is 28.45 percent of the fundamental, while WTHD is 16.61 percent of the fundamental.

Table 1: Switching order of the two-level dual VSI for a multi-level outcome

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Sector | Switching Order-01 | | | | | | |
| I | V0 | V1 | V2 | V0' | V2 | V1 | V0 |
| 0000000 | 1100001 | 1110001 | 1111111 | 1110001 | 1100001 | 0000000 |
| VIII | V0' | V8' | V9' | V0 | V9' | V8' | V0' |
| 1111111 | 0011110 | 0001110 | 0000000 | 0001110 | 0011110 | 1111111 |
| II | V0 | V3 | V2 | V0' | V2 | V3 | V0 |
| 0000000 | 1110000 | 1110001 | 1111111 | 1110001 | 1110000 | 0000000 |
| IX | V0' | V10' | V9' | V0 | V9' | V10' | V0' |
| 1111111 | 0001111 | 0001110 | 0000000 | 0001110 | 0001111 | 1111111 |
| III | V0 | V3 | V4 | V0' | V4 | V3 | V0 |
| 0000000 | 1110000 | 1111000 | 1111111 | 1111000 | 1110000 | 0000000 |
| X | V0' | V10' | V11' | V0 | V11' | V10' | V0' |
| 1111111 | 0001111 | 0000111 | 0000000 | 0000111 | 0001111 | 1111111 |
| IV | V0 | V5 | V4 | V0' | V4 | V5 | V0 |
| 0000000 | 0111000 | 1111000 | 1111111 | 1111000 | 0111000 | 0000000 |
| XI | V0' | V12' | V11' | V0 | V11' | V12' | V0' |
| 1111111 | 1000111 | 0000111 | 0000000 | 0000111 | 1000111 | 1111111 |
| V | V0 | V5 | V6 | V0' | V6 | V5 | V0 |
| 0000000 | 0111000 | 0111100 | 1111111 | 0111100 | 0111000 | 0000000 |
| XII | V0' | V12' | V13' | V0 | V13' | V12' | V0' |
| 1111111 | 1000111 | 1000011 | 0000000 | 1000011 | 1000111 | 1111111 |
| VI | V0 | V7 | V6 | V0' | V6 | V7 | V0 |
| 0000000 | 0011100 | 0111100 | 1111111 | 0111100 | 0011100 | 0000000 |
| XIII | V0' | V14' | V13' | V0 | V13' | V14' | V0' |
| 1111111 | 1100011 | 1000011 | 0000000 | 1000011 | 1100011 | 1111111 |
| VII | V0 | V7 | V8 | V0' | V8 | V7 | V0 |
| 0000000 | 0011100 | 0011110 | 1111111 | 0011110 | 0011100 | 0000000 |
| XIV | V0' | V14' | V1' | V0 | V1' | V14' | V0' |
| 1111111 | 1100011 | 1100001 | 0000000 | 1100001 | 1100011 | 1111111 |
| VIII | V0 | V9 | V8 | V0' | V8 | V9 | V0 |
| 0000000 | 0001110 | 0011110 | 1111111 | 0011110 | 0001110 | 0000000 |
| I | V0' | V2' | V1' | V0 | V1' | V2' | V0' |
| 1111111 | 1110001 | 1100001 | 0000000 | 1100001 | 1110001 | 1111111 |
| IX | V0 | V9 | V10 | V0' | V10 | V9 | V0 |
| 0000000 | 0001110 | 0001111 | 1111111 | 0001111 | 0001110 | 0000000 |
| II | V0' | V2' | V3' | V0 | V3' | V2' | V0' |
| 1111111 | 1110001 | 1110000 | 0000000 | 1110000 | 1110001 | 1111111 |
| X | V0 | V11 | V10 | V0' | V10 | V11 | V0 |
| 0000000 | 0000111 | 0001111 | 1111111 | 0001111 | 0000111 | 0000000 |
| III | V0' | V4' | V3' | V0 | V3' | V4' | V0' |
| 1111111 | 1111000 | 1110000 | 0000000 | 1110000 | 1111000 | 1111111 |
| XI | V0 | V11 | V12 | V0' | V12 | V11 | V0 |
| 0000000 | 0000111 | 1000111 | 1111111 | 1000111 | 0000111 | 0000000 |
| IV | V0' | V4' | V5' | V0 | V5' | V4' | V0' |
| 1111111 | 1111000 | 0111000 | 0000000 | 0111000 | 1111000 | 1111111 |
| XII | V0 | V13 | V12 | V0' | V12 | V13 | V0 |
| 0000000 | 1000011 | 1000111 | 1111111 | 1000111 | 1000011 | 0000000 |
| V | V0' | V6' | V5' | V0 | V5' | V6' | V0' |
| 1111111 | 0111100 | 0111000 | 0000000 | 0111000 | 0111100 | 1111111 |
| XIII | V0 | V13 | V14 | V0' | V14 | V13 | V0 |
| 0000000 | 1000011 | 1100011 | 1111111 | 1100011 | 1000011 | 0000000 |
| VI | V0' | V6' | V7' | V0 | V7' | V6' | V0' |
| 1111111 | 0111100 | 0011100 | 0000000 | 0011100 | 0111100 | 1111111 |
| XIV | V0 | V1 | V14 | V0' | V14 | V1 | V0 |
| 0000000 | 1100001 | 1100011 | 1111111 | 1100011 | 1100001 | 0000000 |
| VII | V0' | V8' | V7' | V0 | V7' | V8' | V0' |
| 1111111 | 0011110 | 0011100 | 0000000 | 0011100 | 0011110 | 1111111 |

Table 2: Switching order of the two-level twin VSI for a multi-level outcome

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Sector | Switching Order-02 | | | | | | |
| I | V0 | V1 | V2 | V0' | V2 | V1 | V0 |
| 0000000 | 1100001 | 1110001 | 1111111 | 1110001 | 1100001 | 0000000 |
| XII | V0 | V13' | V12' | V0' | V12' | V13' | V0 |
| 0000000 | 1000011 | 1000111 | 1111111 | 1000111 | 1000011 | 0000000 |
| II | V0 | V3 | V2 | V0' | V2 | V3 | V0 |
| 0000000 | 1110000 | 1110001 | 1111111 | 1110001 | 1110000 | 0000000 |
| XI | V0 | V11' | V12' | V0' | V12' | V11' | V0 |
| 0000000 | 0000111 | 1000111 | 1111111 | 1000111 | 0000111 | 0000000 |
| III | V0 | V3 | V4 | V0' | V4 | V3 | V0 |
| 0000000 | 1110000 | 1111000 | 1111111 | 1111000 | 1110000 | 0000000 |
| X | V0 | V11' | V10' | V0' | V10' | V11' | V0 |
| 0000000 | 0000111 | 0001111 | 1111111 | 0001111 | 0000111 | 0000000 |
| IV | V0 | V5 | V4 | V0' | V4 | V5 | V0 |
| 0000000 | 0111000 | 1111000 | 1111111 | 1111000 | 0111000 | 0000000 |
| IX | V0 | V9' | V10' | V0' | V10' | V9' | V0 |
| 0000000 | 0001110 | 0001111 | 1111111 | 0001111 | 0001110 | 0000000 |
| V | V0 | V5 | V6 | V0' | V6 | V5 | V0 |
| 0000000 | 0111000 | 0111100 | 1111111 | 0111100 | 0111000 | 0000000 |
| VIII | V0 | V9' | V8' | V0' | V8' | V9' | V0 |
| 0000000 | 0001110 | 0011110 | 1111111 | 0011110 | 0001110 | 0000000 |
| VI | V0 | V7 | V6 | V0' | V6 | V7 | V0 |
| 0000000 | 0011100 | 0111100 | 1111111 | 0111100 | 0011100 | 0000000 |
| VII | V0 | V7' | V8' | V0' | V8' | V7' | V0 |
| 0000000 | 0011100 | 0011110 | 1111111 | 0011110 | 0011100 | 0000000 |
| VII | V0 | V7 | V8 | V0 | V8 | V7 | V0 |
| 0000000 | 0011100 | 0011110 | 1111111 | 0011110 | 0011100 | 0000000 |
| VI | V0 | V7' | V6' | V0' | V6' | V7' | V0 |
| 0000000 | 0011100 | 0111100 | 1111111 | 0111100 | 0011100 | 0000000 |
| VIII | V0 | V9 | V8 | V0' | V8 | V9 | V0 |
| 0000000 | 0001110 | 0011110 | 1111111 | 0011110 | 0001110 | 0000000 |
| V | V0 | V5' | V6' | V0' | V6' | V5' | V0 |
| 0000000 | 0111000 | 0111100 | 1111111 | 0111100 | 0111000 | 0000000 |
| IX | V0 | V9 | V10 | V0' | V10 | V9 | V0 |
| 0000000 | 0001110 | 0001111 | 1111111 | 0001111 | 0001110 | 0000000 |
| IV | V0 | V5' | V4' | V0' | V4' | V5' | V0 |
| 0000000 | 0111000 | 1111000 | 1111111 | 1111000 | 0111000 | 0000000 |
| X | V0 | V11 | V10 | V0' | V10 | V11 | V0 |
| 0000000 | 0000111 | 0001111 | 1111111 | 0001111 | 0000111 | 0000000 |
| III | V0 | V3' | V4' | V0' | V4' | V3' | V0 |
| 0000000 | 1110000 | 1111000 | 1111111 | 1111000 | 1110000 | 0000000 |
| XI | V0 | V11 | V12 | V0' | V12 | V11 | V0 |
| 0000000 | 0000111 | 1000111 | 1111111 | 1000111 | 0000111 | 0000000 |
| II | V0 | V3' | V2' | V0' | V2' | V3' | V0 |
| 0000000 | 1110000 | 1110001 | 1111111 | 1110001 | 1110000 | 0000000 |
| XII | V0 | V13 | V12 | V0' | V12 | V13 | V0 |
| 0000000 | 1000011 | 1000111 | 1111111 | 1000111 | 1000011 | 0000000 |
| I | V0 | V1' | V2' | V0' | V2' | V1' | V0 |
| 0000000 | 1100001 | 1110001 | 1111111 | 1110001 | 1100001 | 0000000 |
| XIII | V0 | V13 | V14 | V0' | V14 | V13 | V0 |
| 0000000 | 1000011 | 1100011 | 1111111 | 1100011 | 1000011 | 0000000 |
| XIV | V0 | V1' | V14' | V0' | V14' | V1' | V0 |
| 0000000 | 1100001 | 1100011 | 1111111 | 1100011 | 1100001 | 0000000 |
| XIV | V0 | V1 | V14 | V0' | V14 | V1 | V0 |
| 0000000 | 1100001 | 1100011 | 1111111 | 1100011 | 1100001 | 0000000 |
| XIII | V0 | V13' | V14' | V0' | V14' | V13' | V0 |
| 0000000 | 1000011 | 1100011 | 1111111 | 1100011 | 1000011 | 0000000 |

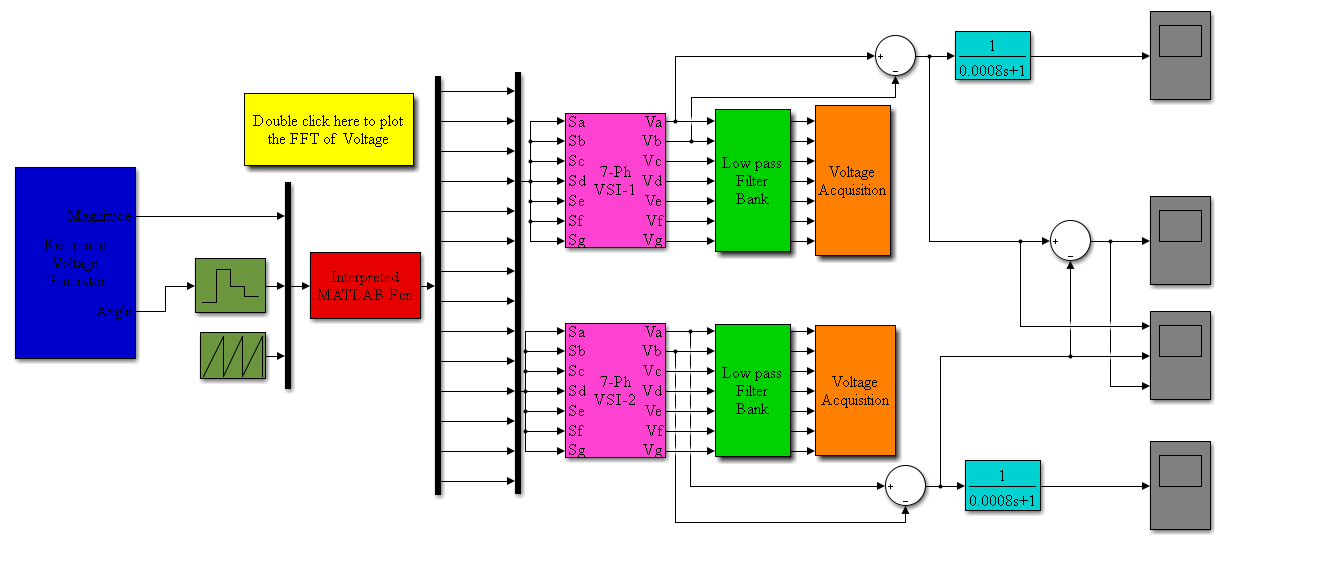


Fig.3.MATLAB/SIMULINK model for three-level operation of a two-level seven-phase dual voltage source inverter

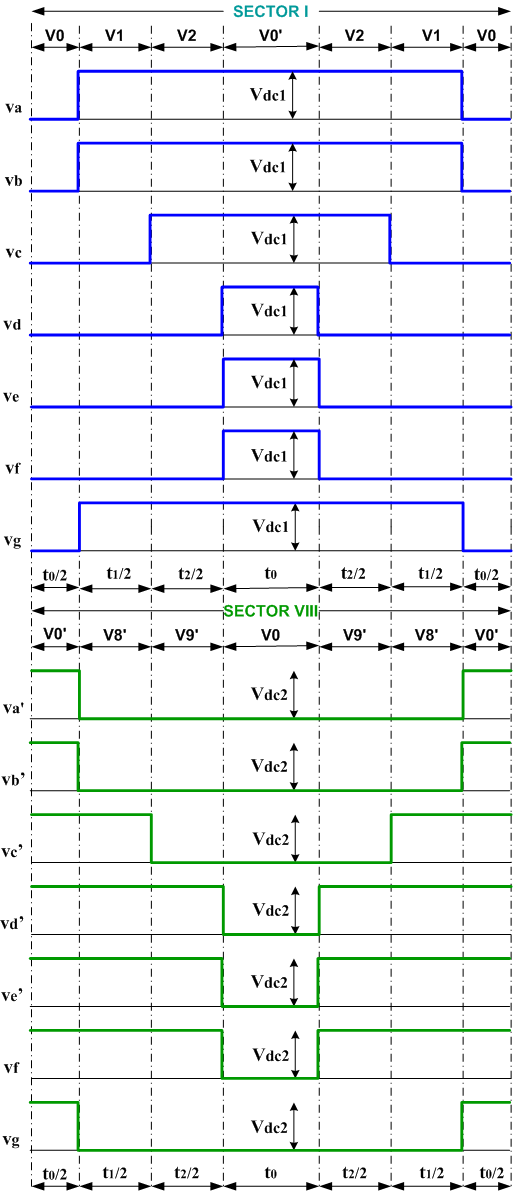


Fig. 1. Switching pattern-01of twin two-level VSI for multi-level outcome

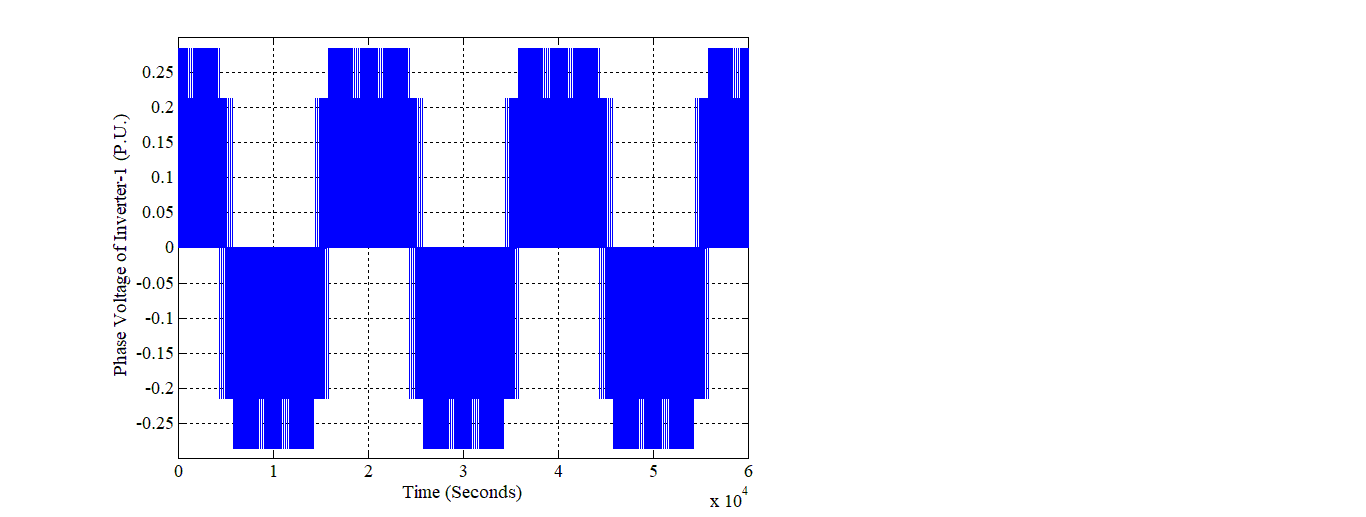


Fig. 4(a). Phase voltage of inverter-1

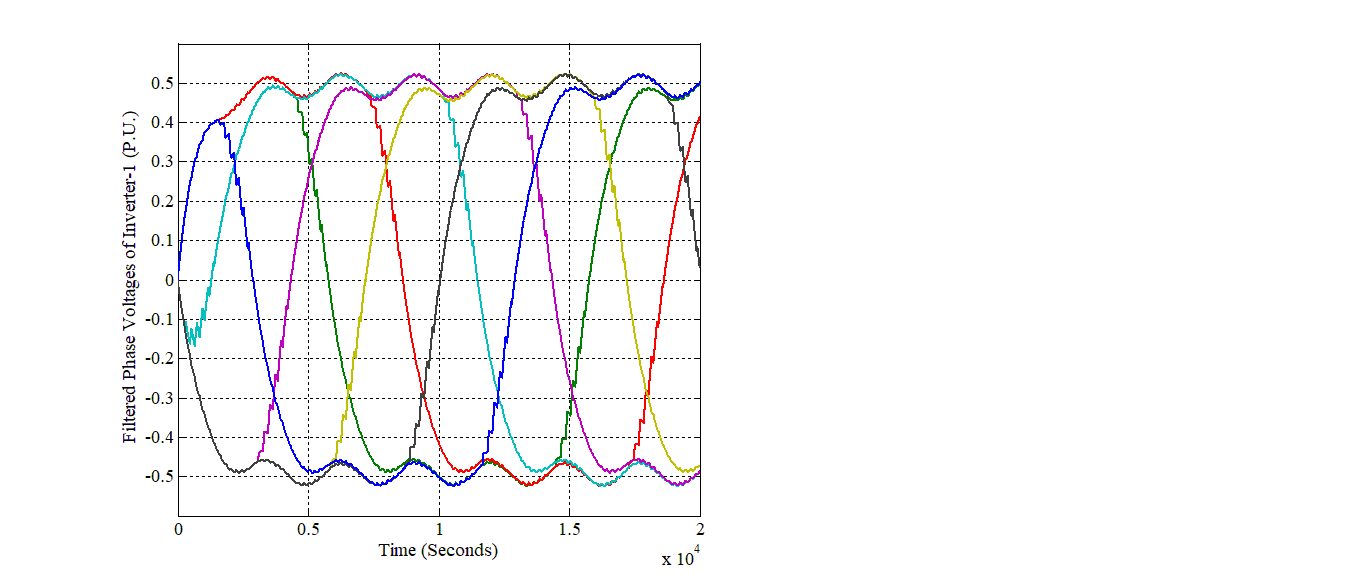


Fig. 5(a). Filtered phase voltages of inverter-1

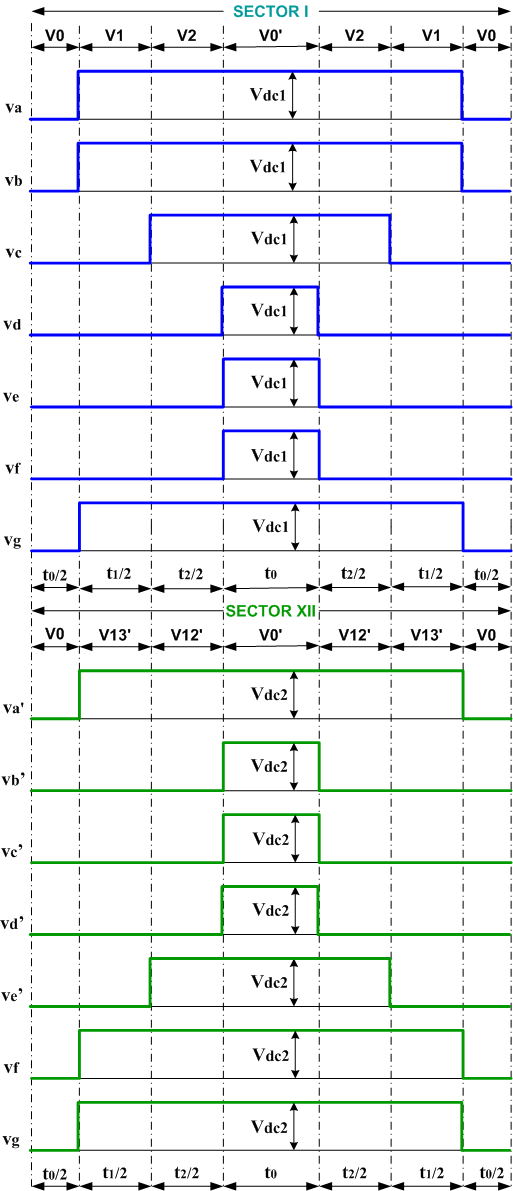


Fig. 2.Switching pattern-02 of twin two-level VSI for multi-level outcome

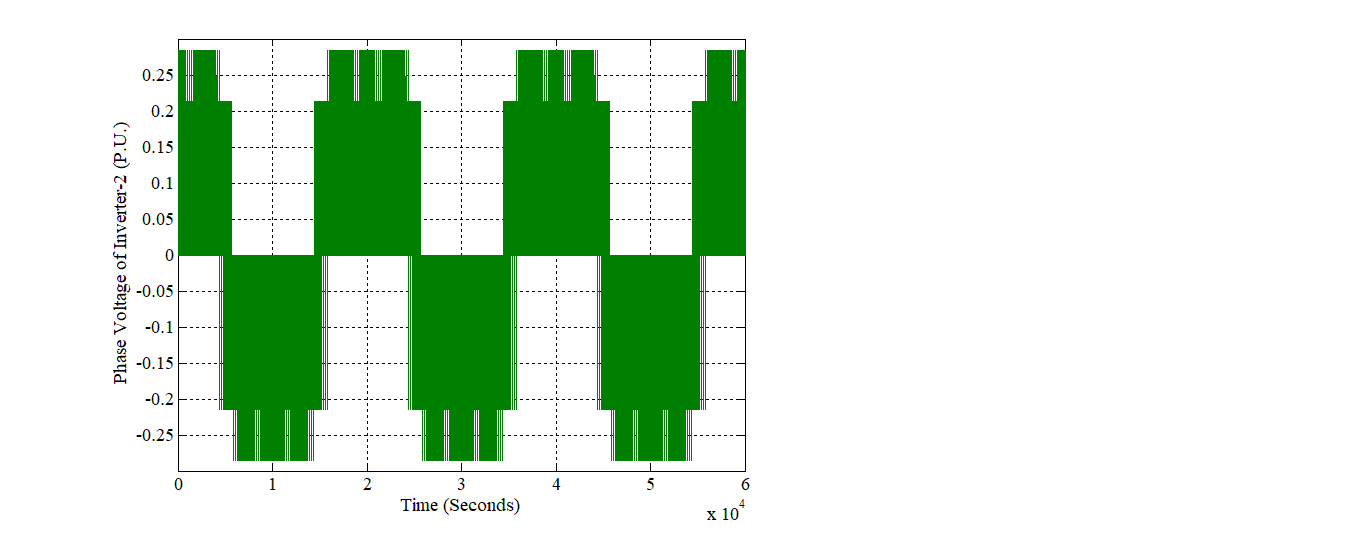


Fig. 4(b). Phase voltage of inverter-2

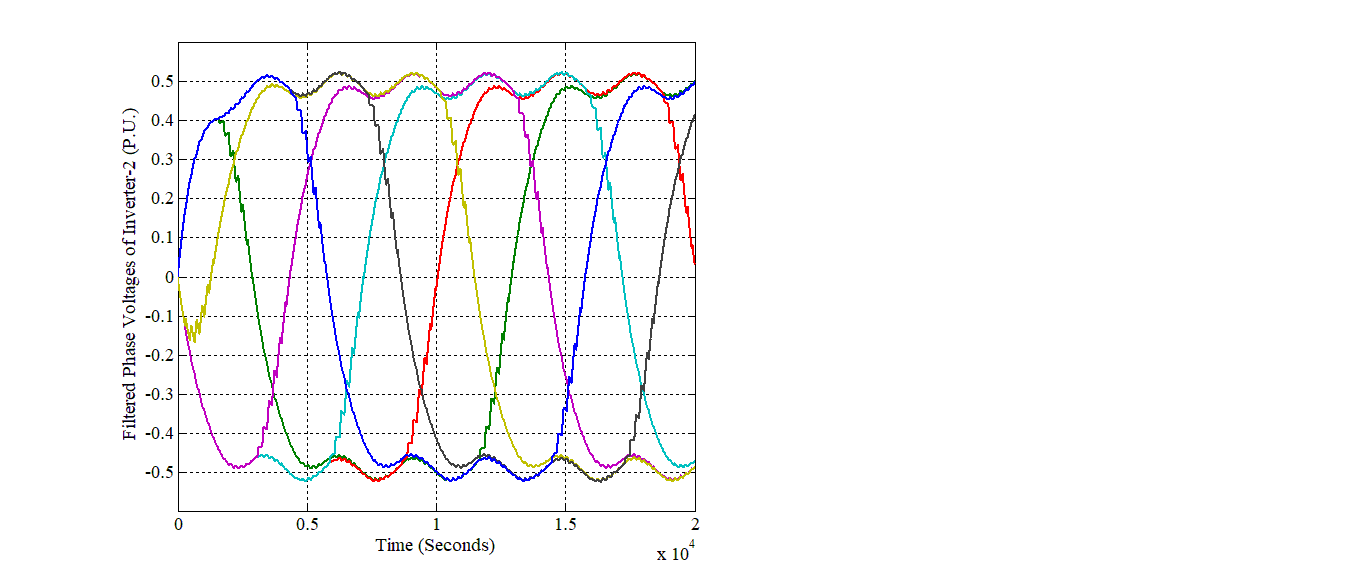


Fig. 5(b). Filtered phase voltages of inverter-2

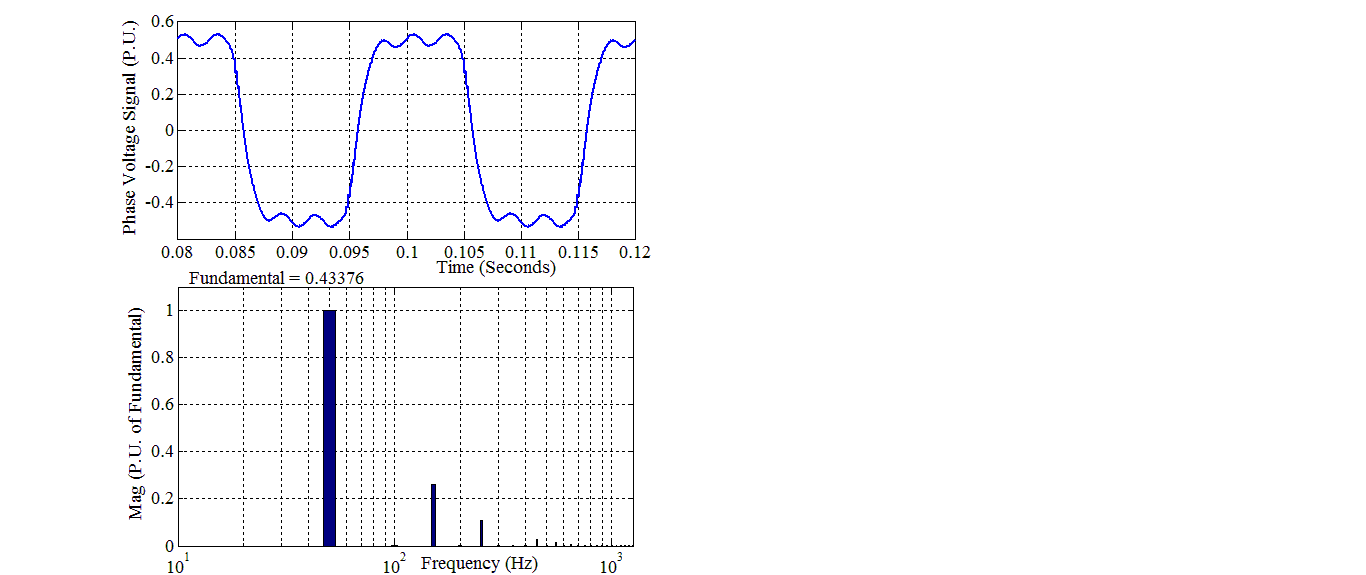


Fig. 6. Harmonic spectrum for phase voltage ‘a’at 5k switching frequency

# Conclusion

The space vector pulse width modulation technique employing only large vectors is suggested in this work for a two-level seven-phase dual voltage source inverter for multi-level outcome. Because only large vectors were utilized to execute the method, the resultant system output is notprecisely sinusoidal. Both SVPWM technique has been tried and proven practical, and simple to apply. Experimental testing will be done in the future to have a better understanding. The suggested methods is more suited to high-power applications such as electric cars, which require two separate isolated dc sources.

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